A Self-Boost Charge Pump Topology for a Gate Drive High-Side Power Supply

Shihong Park, *Student Member, IEEE,* and Thomas M. Jahns, *Fellow, IEEE*

***Abstract*—A self-boost charge pump topology is presented for a floating high-side gate drive power supply that features high voltage and current capabilities for use in integrated power electronic modules (IPEMs). The transformerless topology uses a small capacitor to transfer energy to the high-side switch from a single power supply referred to the negative rail. Unlike conventional bootstrap power supplies, no switching of the main phase-leg switches is required to provide power continuously to the high-side gate drive, even if the high-side switch is permanently on. Additional advantages include low parts-count and simple control requirements. A piecewise linear model of the self-boost charge pump is derived and the circuit's operating characteristics are analyzed. Simulation and experimental results are provided to verify the desired operation of the new charge pump circuit. Guidelines are provided to assist with circuit component selection in new applications.**

***Index Terms*—Bootstrap power supply, floating, high-side gate drive, MOS-gated power semiconductors, power module, transformerless.**

I. Introduction

A. Background

BOOTSTRAP circuits are widely used in bridge inverters to provide the floating power supply for high-side switch gate drives [1]. They are often preferred over high-frequency transformer circuits due to their simplicity and basic compatibility with integrated circuit implementation, making them well suited for achieving low cost and high reliability.

However, the bootstrap technique imposes significant limitations due to its periodic charging time requirements that can interfere with the desired gate drive operation under some important operating conditions [1]. In particular, the high-side gate drive can become starved of energy if the inverter switching algorithm calls for either switch to be on for long intervals. Under such circumstances, the main phase-leg switch may be forced to perform a brief switching cycle in order to refresh the depleted capacitor charge for the high-side gate drive.

One approach that has been proposed to overcome these problems uses an auxiliary charge pump [2]–[4]. This technique can provide the needed power for a high-side gate drive without interfering with the desired phase-leg switching sequence. However, it is not widely used due to its higher complexity and its requirements for high-voltage level shifting to supply control signals to the auxiliary switches.

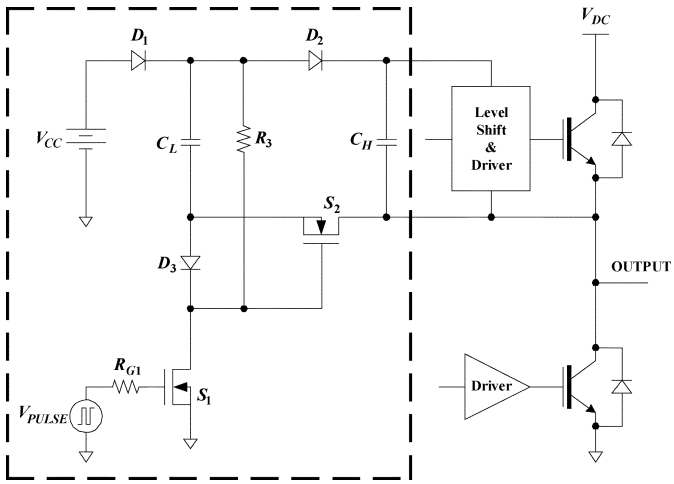

Fig. 1. Self-boost charge pump circuit configuration for an inverter phase leg high-side power supply.

Another technique has been described in the literature [5], [6] that applies charge pump techniques to deliver power to a floating high-side power supply. It has a simple topology and overcomes the limitation of conventional bootstrap high-side power supplies by transferring charge even when the upper switch is permanently on. However, this technique suffers in high current applications from high power losses in the charge pump oscillator and high voltage ripple due to large voltage surges caused by switching of the main phase-leg switches. These disadvantages limit this technique to gate drive applications with low current supply requirements.

A new charge pump topology is presented in this paper for floating high-side gate drive power supplies that avoid the problems of existing techniques while retaining the advantages of simplicity and compatibility with integrated circuit implementation. This topology, shown in Fig. 1 with a standard inverter phase leg, uses a modified charge-pump circuit to deliver power from the low side to the high side.

B. Operating Principles

The operation of this new charge-pump circuit can be divided into the following three modes: charging, boost, and pumping modes. Each mode will be described individually assuming that the upper phase-leg switch is on. Under these conditions, the potential of the output node is nearly $V_{\rm dc}$. For convenience, the

Manuscript received March 31, 2003; revised August 18, 2004. This work was supported by the ERC Program of the U.S. National Science Foundation under Award EEC-9731677 and by the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). Recommended by Associate Editor F. Blaabjerg.

S. Park is with the School of Electrical, Electronics, and Computer Engineering, Dankook University, Seoul 140-714, Korea (e-mail: shihong@dankook.ac.kr).

T. M. Jahns is with the University of Wisconsin-Madison, Madison, WI 53706 USA (e-mail: t.jahns@ieee.org).

Digital Object Identifier 10.1109/TPEL.2004.843013

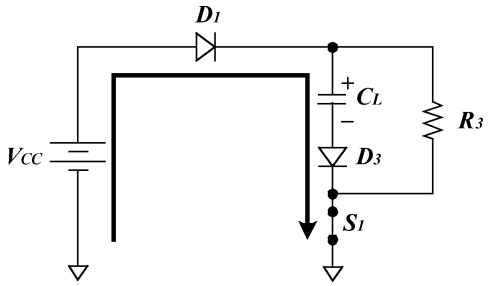

Fig. 2. Charging mode (S_1 is on and S_2 is off).

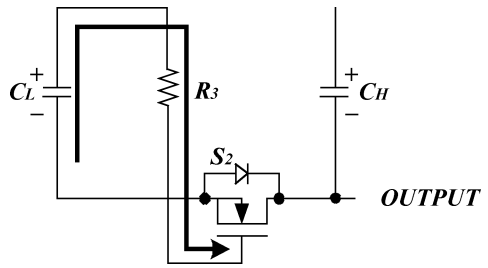

Fig. 3. Boost mode (S_1 is off and S_2 is active).

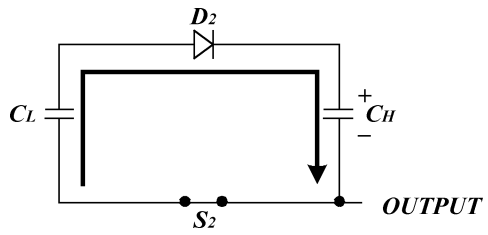

Fig. 4. Pumping mode (S_1 is off and S_2 is on).

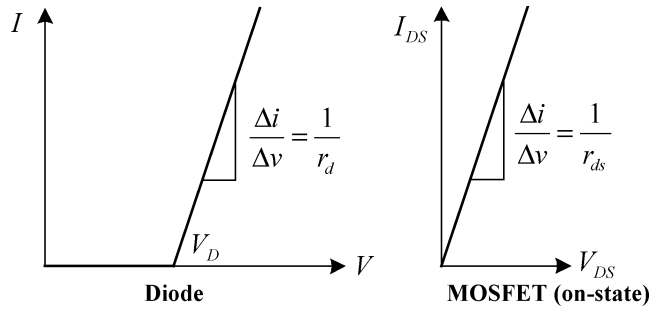

Fig. 5. Linearized diode and MOSFET models.

negative rail is considered to be ground potential in the following description.

Charging Mode (Fig. 2): The boost capacitor C_L in Fig. 1 is charged by the single low-side power supply $V_{\rm CC}$ through D_1 and D_3 when the switch S_1 turns on as shown in Fig. 2. S_2 and D_2 remain in their off-states since the gate-source voltage V_{GS2} is forced to $-V_{\rm D3}$ during this charging mode. D_1, D_2, S_1 and S_2 must all be high-voltage devices that can sustain voltages up to the dc link voltage $V_{\rm dc}$. D_3 can be a low-voltage diode because its maximum reverse voltage is limited by the voltage on C_L which is lower than $V_{\rm CC}$. A Schottky diode is preferred for D_3 in order to minimize its voltage drop and the resulting conduction losses.

Boost Mode (Fig. 3): When S_1 turns off, the voltage V_L on the boost capacitor C_L starts to charge the gate capacitance of S_2, $C_{\rm GATE}$, through R_3. Assuming that C_L is much bigger than $C_{\rm GATE}$, the decrease in the C_L voltage V_L is negligible. The value of R_3 determines the turn-on time of S_2, but does not affect the magnitude of the final S_2 gate voltage. Once $C_{\rm GATE}$ is charged, there is no additional current flow or loss in R_3.

The voltage at the negative (lower) terminal of C_L rises from ground level to $V_{\rm dc}$ (the output node voltage) as switch S_1 turns off and the drain-source voltage of S_2 decreases as shown in Fig. 3.

Pumping Mode (Fig. 4): After S_2 fully turns on, the charge in the boost capacitor C_L is transferred to the high-side capacitor C_H that serves as the local supply for the high-side switch gate. This pumping mode ends when S_1 is turned on again by the external control. Continuous switching of S_1 insures that gate drive charge is available at all times to the high-side switch without any interference with the desired phase-leg switching sequence.

C. Paper Organization

Models for each of the three modes are analyzed in Section II using linearized diode and metal oxide semiconductor field effect transistor (MOSFET) models that include the effects of load current. For high voltage applications, the voltage drops caused by the internal resistances of the diodes and MOSFETs become progressively more significant as their current levels increase. Steady-state operation is also analyzed, illuminating the effects of important parameters including frequency, duty cycle, delay times, and switching times. Following this analysis, simulation and experimental results are presented in Section III to verify the model and to demonstrate the circuit's operating characteristics.

II. Charge Pump Circuit Analysis

Fig. 5 shows the voltage-current characteristics of a common piecewise-linear model for diodes and on-state MOSFETs that will be used in this simplified analysis. The V-I characteristics of the diode can be defined by two parameters—the voltage drop V_D and the on-state resistance r_d.

As note above, a Schottky diode is a good choice for D_3 in order to minimize its forward voltage drop. The Schottky diode forward voltage is typically 0.1∼0.2 V, while the comparable voltage for a standard silicon junction diode is 0.7 V.

The MOSFET will be modeled as a simple resistor r_{ds} after it turns on as shown in Fig. 5. The reverse leakage current of the MOSFET and diode are ignored in this analysis. IGBT's could be used instead of MOSFETs for a high-voltage application (>600 V), but the forward voltage drop of an IGBT is typically higher than that of a MOSFET for low current conditions.

The voltage waveforms across each low-side and high-side capacitor during the three operating modes are shown in Fig. 6 for initial start-up operation. The fixed-frequency input control signal $V_{\rm PULSE}$ and the switch S_1 drain-source voltage $V_{\rm DS1}$ are also shown to help explain the circuit's operation.

The equations for the boost capacitor C_L voltage $V_L(t)$ and the high-side capacitor C_H voltage $V_H(t)$ will be analyzed for each of the three operating modes using equivalent circuits. The value of $V_H(t)$ under steady-state conditions will also be calcu-

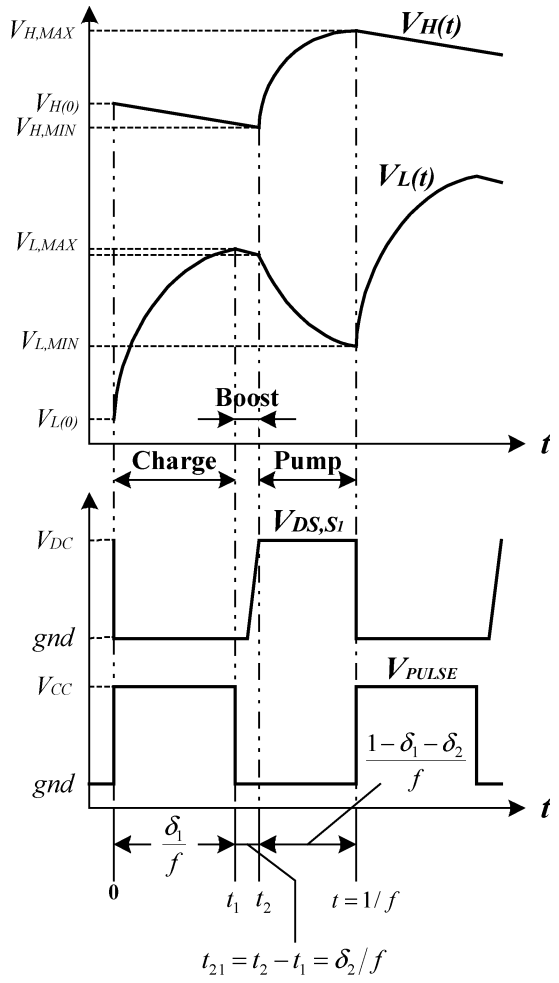

Fig. 6. Self-boost charge pump waveforms during initial start-up operation.

lated as a function of the boost time t_{21} to illustrate the control principles for the new charge-pump circuit.

A. Charging Mode Equivalent Circuit and Analysis

During the charging mode, switch S_1 is on and switch S_2 is in its off state. The boost capacitor C_L is charged through D_1, D_3 and S_1. The equivalent circuit for the charging mode is shown in Fig. 7. The maximum charging voltage of C_L is $V_{\mathrm{L,MAX}} = V_{\mathrm{CC}} - V_{\mathrm{D1}} - V_{\mathrm{D3}}$ and the equivalent resistor value is $R_{EQ} = r_{\mathrm{d1}} + r_{\mathrm{d3}} + r_{\mathrm{dS1}}$. The boost capacitor voltage $V_L(t)$ during the charging mode can be calculated as

$$v_L(t) = v_L(0) + [V_{\mathrm{L,MAX}} - v_L(0)]\left(1 - e^{\frac{-t}{R_{EQ}\cdot C_L}}\right). \quad (1)$$

It is worth noting that the same voltage $V_{\mathrm{L,MAX}}$ (plus the D_3 diode drop) appears across resistor R_3 during the charging mode, resulting in power dissipation in R_3 during this interval.

B. Boost Mode Equivalent Circuit and Analysis

During the boost mode, S_1 turns off, D_3 transitions to its off-state, and the gate capacitance of S_2 is charged so S_2 begins to turn on. Fig. 8 shows the equivalent circuit during this operating mode. The time constant of the exponential voltage increase is

$$\tau_{\mathrm{Boost}} = R_3 \frac{C_L C_{\mathrm{GATE}}}{C_L + C_{\mathrm{GATE}}} \quad (2)$$

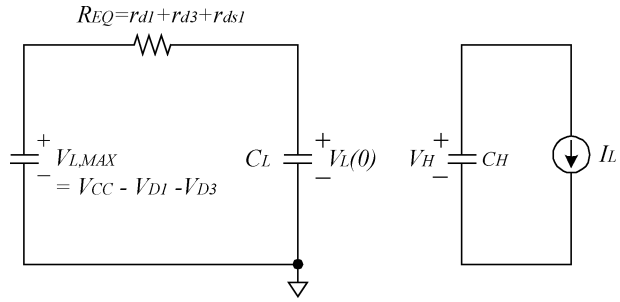

Fig. 7. Charging mode model.

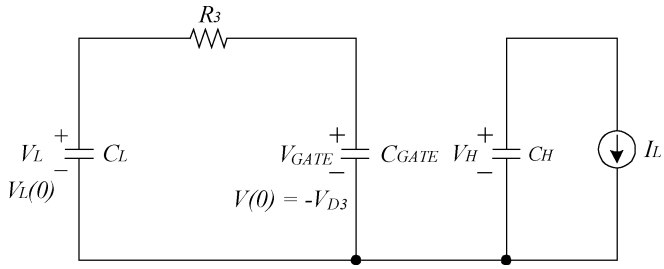

Fig. 8. Boost mode model.

where C_{GATE} is the total gate capacitance of S_2.

The voltage on both C_L and C_{GATE} following completion of this gate-charging interval is

$$V_L = \frac{C_L \cdot V_L(0)}{C_L + C_{\mathrm{GATE}}}. \quad (3)$$

It is evident in (3) that if C_L is much bigger than C_{GATE}, the voltage decrease of C_L compared to its initial value $V_L(0)$ is negligible, and the value of R_3 does not affect the final voltage value.

The load on the gate drive circuit is modeled by a constant load current I_L that flows at all times. The floating high-side capacitor C_H is discharged by this load current I_L during both the charging and boost modes. Thus, the equation for the high-side capacitor voltage V_H during the boost mode can be expressed simply as

$$V_H(t) = V_H(0) - \frac{I_L}{C_H} \cdot t. \quad (4)$$

C. Pumping Mode Equivalent Circuit and Analysis

The pumping mode begins when S_2 fully turns on while S_1 remains off. The equivalent circuit for this pumping mode is shown in Fig. 9, where the equivalent resistance R_{EQ2} consists of the series combination of the equivalent resistances of diode $D_2(r_{\mathrm{d2}})$ and switch $S_2(r_{ds2})$. The high-side capacitor voltage V_H can be derived as

$$V_H(t) = V_H(0)e^{\frac{-t}{\tau}} + \frac{C_L V_L'(0) + C_H V_H(0)}{C_L + C_H}\left(1 - e^{\frac{-t}{\tau}}\right) - \frac{R_{\mathrm{EQ2}} C_L^2 I_L}{(C_L + C_H)^2}\left(1 - e^{\frac{-t}{\tau}}\right) - \frac{I_L}{C_L + C_H}t \quad (5)$$

$$\text{where} \qquad \tau = R_{\mathrm{EQ2}} \frac{C_L C_H}{C_L + C_H} \quad (6)$$

$$R_{\mathrm{EQ2}} = r_{\mathrm{d2}} + r_{ds2} \quad (7)$$

$$V_L'(0) = V_L(0) - V_{\mathrm{D2}}. \quad (8)$$

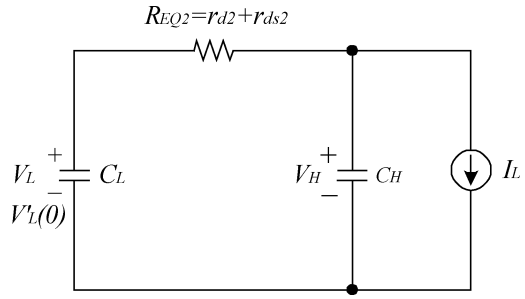

Fig. 9. Pumping mode model.

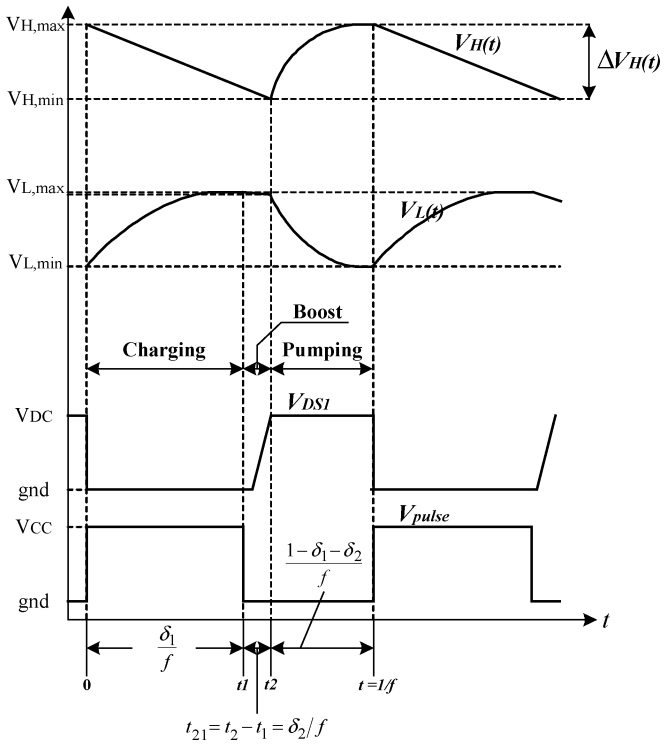

Fig. 10. Self-boost charge pump waveforms during steady-state operation.

The second term in (5) represents the stored capacitor charge in C_L that is transferred from the low-side supply to the high-side gate drive. The third and fourth terms represent the voltage drops due to the equivalent resistor and the gate drive load current, respectively.

D. V_H Under Steady-State Conditions

Under steady-state conditions, the maximum and minimum voltage levels of V_H and V_L remain constant as shown in Fig. 10. Applying the steady-state constraints, the minimum value of the high-side capacitor voltage during steady-state conditions $V_{H,MIN}$ can be expressed as

$$V_{H,MIN} = V_{\mathrm{H,MAX}} - \Delta V_H \tag{9}$$

$$\text{where} \quad \Delta V_H = \frac{I_L}{C_H}\frac{\delta_1 + \delta_2}{f} \tag{10}$$

and the duty cycle values during the charging and boost intervals are δ_1 and δ_2, respectively (see Fig. 10).

In (9), the second term represents the ripple voltage amplitude ΔV_H. In order to reduce the ripple voltage amplitude, either the value of the high-side capacitance C_H must be increased or a higher frequency f is required. However, the switching losses in switches S_1 and S_2 make it undesirable to raise the frequency too high. Reducing the duty cycle interval δ_2 makes it possible to transfer more charge from the low to high sides, and this helps to reduce the ripple voltage amplitude. However, it is important to recognize that one of the most direct ways to reduce δ_2 is to lower the value of resistor R_3 which causes higher power dissipation in R_3 during the charging mode. As a result, selection of the R_3 value represents of the significant tradeoffs that must be considered during the circuit design process.

$V_{\mathrm{H,MAX}}$ can be derived starting from (5), defining the duration of the pumping interval as $t_{\mathrm{PUMP}} = (1 - \delta_1 - \delta_2)/f$ (see Fig. 10). If $t_{\mathrm{PUMP}} > 2 \cdot \tau$, the value of the exponential function in this equation is less than 0.14 $(= e^{-2})$. Assuming that this condition is met so that the terms proportional to this exponential can be ignored, (5) can be evaluated at the end of the pumping interval to establish an approximate expression for $V_{\mathrm{H,MAX}}$

$$\begin{aligned} V_{\mathrm{H,MAX}} &= V_H(t_{\mathrm{PUMP}}) \\ &= \frac{C_L V_L'(0) + C_H V_H(0)}{C_L + C_H} - \frac{R_{\mathrm{EQ2}} C_L^2 I_L}{(C_L + C_H)^2} \\ &\quad - \frac{I_L}{C_L + C_H} t_{\mathrm{PUMP}}. \end{aligned} \tag{11}$$

The final expression of $V_{\mathrm{H,MAX}}$ can be derived using the following two initial conditions at the beginning of the pumping stage using the previously-defined variable $V_{\mathrm{L,MAX}}$ and (9) and (10)

$$\begin{aligned} V_L'(0) &= V_{\mathrm{L,MAX}} - V_{\mathrm{D2}} \\ &= V_{\mathrm{CC}} - V_{\mathrm{D1}} - V_{\mathrm{D2}} - V_{\mathrm{D3}} \end{aligned} \tag{12}$$

$$\begin{aligned} V_H(0) &= V_{H,MIN} \\ &= V_{\mathrm{H,MAX}} - \frac{I_L}{C_H} \cdot \frac{\delta 1 + \delta 2}{f}. \end{aligned} \tag{13}$$

Substituting these two expressions into (11) and solving for $V_{\mathrm{H,MAX}}$ leads to

$$V_{\mathrm{H,MAX}} = V_{\mathrm{CC}} - V_{\mathrm{D1}} - V_{\mathrm{D2}} - V_{\mathrm{D3}} - \frac{R_{\mathrm{EQ2}} I_L C_L}{C_L + C_H} - \frac{I_L}{C_L f}. \tag{14}$$

Equation (14) is valid only if the durations of the charging and pumping modes are sufficiently long compared to the RC time constants during each of these intervals. If not, the maximum value of V_H decreases and the exact value of $V_{\mathrm{H,MAX}}$ should be calculated using (5). If possible, the time constants in (1) and (6) should be set to values that are small compared to the charging and pumping time intervals for a given frequency condition. Otherwise, the maximum output voltage decreases due to insufficient charging and pumping times. Although this suggests reduced values for C_L and C_H, higher capacitance values are required to minimize the voltage ripple [see (10)] and to increase the maximum value of the output voltage $V_{\mathrm{H,MAX}}$ in (14). This identifies another significant tradeoff that must be addressed during the circuit design process.

E. Calculation of Boost Time t_{21}

As the operating frequency f increases, the effect of the boost time t_{21} (see Fig. 6) on the output voltage is more significant be-

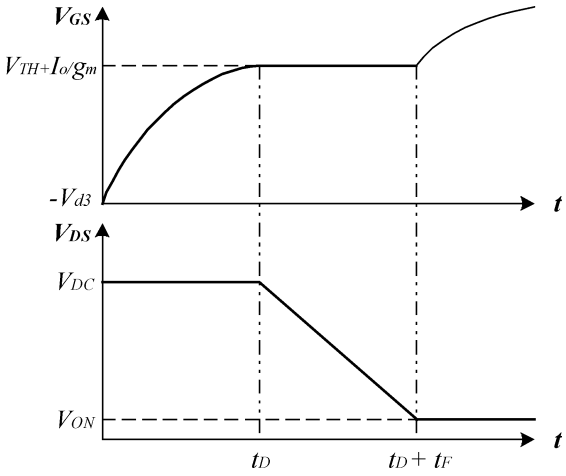

Fig. 11. $V_{\rm GS}$ and V_{DS} waveforms for S_2 during t_{21} boost interval.

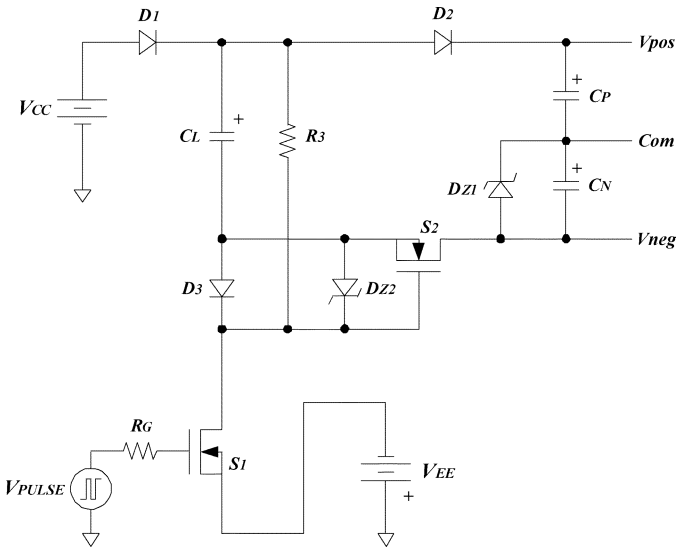

Fig. 12. Modified self-boost charge pump with positive- and negative-bias voltage supply capability.

cause the ratio of charging (pumping) to discharging time values for C_H decreases if t_{21} and duty cycle δ_1 are fixed in value. It should be noted that t_{21} is determined by the boost-mode time constant $\tau_{\rm Boost}$ defined in (2). The duration of the boost mode does not change as the frequency f is varied for a given switch S_2 and a given value of R_3. This makes t_{21} a key parameter under higher frequency conditions since duty cycle δ_2 is directly proportional to the frequency (i.e., $\delta_2 = t_{21} * f$).

Closer examination reveals that the time interval t_{21} can be separated into two subintervals consisting of a delay time t_D and fall time t_F, representing the typical turn-on switching characteristics of S_2 as shown in Fig. 11. During t_D, the gate node is charged up to the threshold voltage $V_{\rm TH}$. At that point, the drain current starts to flow in S_2. V_{DS} falls during t_F while the gate-source voltage $V_{\rm GS}$ remains nearly constant at $V_{\rm TH}$ due to the Miller effect.

The intervals t_D and t_F can be calculated using the circuit and switch model parameters as follows [7]:

$$t_D = R_3 \cdot C_{\rm EQ2} \cdot \ln \frac{V_{\rm CC} - V_{\rm D1} - V_{\rm D2}}{V_{\rm CC} - V_{\rm D1} - 2 \cdot V_{\rm D2} - V_{\rm TH} - \frac{g_m}{I_O}} + R_3 \cdot C_{\rm EQ2} \cdot \ln \frac{V_{\rm CC} - V_{\rm D1} - V_{\rm D2}}{V_{\rm CC} - V_{\rm D1} - V_{\rm D2} - V_{\rm TH}} \quad (15)$$

$$t_F = \frac{V_{\rm dc} \cdot R_3 \cdot C_{\rm GD}}{V_{L(0)} - V_{\rm TH} - \frac{g_m}{I_O}} \quad (16)$$

where

$V_{\rm TH}$ gate threshold voltage $[V]$;
$V_{\rm dc}$ dc link voltage $[V]$;
g_m device transconductance $[A/V]$;
I_o load inductor current $[A]$

$$C_{\rm EQ2} = \frac{C_L \cdot (C_{\rm GD} + C_{\rm GS})}{C_L + C_{\rm GD} + C_{\rm GS}} [F] \quad (17)$$

$C_{\rm GD}$ device gate-drain capacitance $[F]$;
$C_{\rm GS}$ device gate-source capacitance $[F]$.

It should be no surprise that choosing a MOSFET for S_2 that has fast switching characteristics, including low values of $C_{\rm GD}$ and $C_{\rm GS}$, helps to reduce the duration of the boost interval t_{21} by reducing the delay and fall times t_D and t_F. In addition, (15)–(17) indicate that reducing the values of R_3 and C_L also help to reduce t_{21}. However, the performance tradeoffs involved in lowering the values of these two circuit component values have already been noted and will be discussed further in Section II-G.

F. Circuit Modifications for Bipolar Gate Voltages

Negative gate bias is widely used in high-power phase-leg applications in order to prevent dangerous retriggering problems. Fig. 12 shows a modified version of the self-boost charge pump scheme with positive and negative voltage supply capability. Zener diode $D_{\rm Z1}$, positive voltage capacitor C_P, and negative voltage capacitor C_N are used to split the boost capacitor voltage V_L into two parts for the high-side gate drive. The second supply voltage $V_{\rm EE}$ is added to provide negative gate voltage for the low-side switch in the phase leg. The ground terminal in this figure corresponds to the low-side dc bus voltage, consistent with Fig. 1.

During the charging mode, boost capacitor C_L is charged by $V_{\rm CC} + V_{\rm EE}$ in order to develop nearly the same positive and negative voltages ($V_{\rm CC}$ and $V_{\rm EE}$, respectively) in the high-side gate drive. The maximum charging voltage of C_L is $V_{\rm L,MAX,PN} = V_{\rm CC} + V_{\rm EE} - V_{\rm D1} - V_{\rm D3}$. Zener diode $D_{\rm Z2}$ is required to insure that the maximum safe gate-source voltage of S_2 is not exceeded during the boost or pumping modes. During the pumping mode, stored charge in C_L is distributed to both C_P and C_N, with the negative-bias voltage developed across C_N limited by $D_{\rm Z1}$.

The zener diode $D_{\rm Z1}$ should be selected with a clamping voltage $V_{\rm DZ1}$ that is less than $V_{\rm EE}$ in order to maintain a stable negative bias voltage source for the high-side switch under all operating conditions. If the clamping voltage $V_{\rm DZ1}$ is higher than $V_{\rm EE}$, the negative-bias gate voltage for the high-side switch will drop to the lower voltage $V_{\rm EE}$ when the low-side switch is on. This occurs because the Com terminal in Fig. 12, corresponding to the low-side switch collector voltage (see Fig. 1),

falls to nearly ground (i.e., low-side dc bus) potential when the low-side switch is on.

Using (14), approximate expressions for the negative-bias voltage V_N and the maximum positive-bias voltage $V_{\mathrm{P,MAX}}$ under steady-state conditions can be derived as

$$V_N = V_{\mathrm{DZ1}} \tag{18}$$

$$V_{\mathrm{P,MAX}} = V_{\mathrm{CC}} + V_{\mathrm{EE}} - V_{\mathrm{DZ1}} - V_{\mathrm{D1}} - V_{\mathrm{D2}} - V_{\mathrm{D3}} - \frac{R_{\mathrm{EQ2}} I_L C_L}{C_L + C_H} - \frac{I_L}{C_L f}. \tag{19}$$

G. Circuit Design Guidelines

In order to minimize cost and complexity, the high-side power supply uses a simple open-loop control to set the output voltage with a fixed-frequency, fixed duty-cycle switching sequence. The desired output voltage characteristics can be specified in terms of the maximum output voltage and ripple voltage amplitude for a specified load current. These target values for $V_{\mathrm{H,MAX}}$, ΔV_H, and I_L provide the necessary starting points for determining values for the circuit components.

Once these three performance parameters are set, tradeoffs between the sizes of the circuit components (influencing cost) and the circuit losses come to the forefront in determining the circuit component values. This tradeoff is particularly apparent when considering the voltage ripple requirement. Equation (10) indicates that product of C_H and frequency f must be approximately constant in order to achieve a particular value of ripple voltage ΔV_H for the specified load current I_L. (It is assumed that the sum of the duty cycles $(\delta_1 + \delta_2)$ can vary over only a rather narrow range in the vicinity of 0.5.) Increasing capacitance C_H increases the capacitor's size and cost, while raising the frequency f increases the circuit losses because of higher total switching losses in S_1 and S_2.

In addition, increasing frequency f will likely make it necessary to reduce the value of resistor R_3, further increasing circuit losses, as described previously. As a general guideline, the value of R_3 should be chosen so that the boost interval duty cycle δ_2 does not exceed 0.1 at the desired operating frequency. Higher values of δ_2 are likely to unacceptably degrade the charging times for capacitors C_L and C_H during the charging and pumping modes, respectively. The average power loss in R_3 can be calculated approximately by assuming a 50% duty cycle (i.e., $\delta_1 = 0.5$), leading to the following expression:

$$P_{R3} = \frac{(V_{\mathrm{CC}} - V_{\mathrm{D1}})^2}{2 \cdot R_3}. \tag{20}$$

Another factor that must be considered in the process of selecting the operating frequency is the quality of the MOSFET switches S_1 and S_2. Better MOSFETs with lower values of on-state resistance r_{ds}, lower gate capacitance [C_{GATE} in (2)], and faster switching speeds will reduce circuit losses and make it considerably easier to raise the frequency f. However, adoption of such improved devices is likely to increase the MOSFET size and cost.

Ultimately, selection of the frequency depends on the application. For example, if the target application calls for integrating the high-side power supply inside a power module, then minimizing the volume of the capacitor components is likely to be a high priority. In this case, the design approach would likely call for raising the operating frequency as high as possible, limited by the maximum losses that can be safely dissipated inside the module.

Up to this point, it has been assumed that the value of the charging mode duty cycle δ_1 is 0.5. This is a reasonable choice because of the need to charge and discharge low-side capacitor C_L each cycle. In fact, a simple timer circuit may force δ_1 to be fixed at 0.5. However, further tuning the value of δ_1 (when practical) may yield some improvement in circuit performance by providing a means to compensate for the impact of the boost duty cycle δ_2 and differences between the time constants for the charging and pumping intervals [see (1) and (5)].

The selection of capacitance of C_L also involves tradeoffs between competing objectives of performance and size/cost. In particular, increasing capacitance C_L tends to increase the peak value of the output voltage $V_{\mathrm{H,MAX}}$ for a given value of supply voltage V_{CC} because of the importance of the last term in (14). The penalty is a larger capacitor. Considering these tradeoffs, a good starting point is to choose C_L and C_H to be equal in value, resulting in time constants for the C_L charging and discharging (i.e., pumping) intervals that have similar values.

Assuming that the conditions are met for (14) to give a good approximation of $V_{\mathrm{H,MAX}}$, (14) can be used to eliminate load current I_L and frequency f from the expression. If one accepts the observation that the next-to-last term in (14) can typically be ignored because it is small compared to all of the others, the equation can be rearranged to yield an approximate expression for the supply voltage V_{CC} needed to achieve the specified $V_{\mathrm{H,MAX}}$ value

$$V_{\mathrm{CC}} \cong V_{\mathrm{H,MAX}} + V_{\mathrm{D1}} + V_{\mathrm{D2}} + V_{\mathrm{D3}} + \frac{C_H}{C_L} \frac{\Delta V_H}{(\delta_1 + \delta_2)}. \tag{21}$$

III. Simulation and Experimental Results

Simulations and experimental tests were carried out to verify the operation of the self-boost charge pump circuit. Fig. 13 shows the test circuit that was used for the laboratory tests. The simulations have been carried out using PSPICE with the same test circuit. The devices used for the switches S_1 and S_2 are both the same MOSFET type BUZ50B manufactured by Infineon and rated at 1000 V and 3 A. Diode types 1N4007 and 1N5818 were selected for the high-voltage diode D_2 and the low-voltage Schottky diode D_3, respectively. The reverse blocking voltage of the 1N4007 diode is 1000 V, the same as the MOSFET voltage rating.

The test conditions used for both the experimental tests and the simulations are as

$$V_{\mathrm{dc}} = 600\ \mathrm{V} \quad V_{\mathrm{CC}} = 20\ \mathrm{V} \quad f = 5\ \mathrm{kHz} \quad \delta_1 = 0.5$$
$$C_L = 10\ \mu\mathrm{F} \quad C_H = 10\ \mu\mathrm{F} \quad R_g = 2\ \mathrm{k}\Omega \quad R_o = 600\ \Omega.$$
$$R_3 = 2\ \mathrm{k}\Omega$$

The value of R_o was set to 600 Ω to adjust the load current to approximately 28 mA for a V_H value of 17 V. This resistor represents an average load of 476 mW imposed by the high-side switch gating. For reference, this power level would be sufficient for use with commercially-available gate drive ICs to drive a

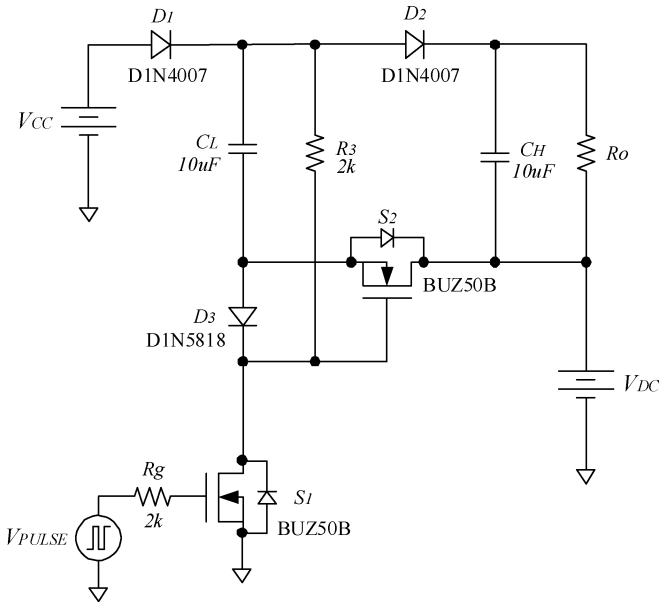

Fig. 13. Self-boost charge pump test circuit.

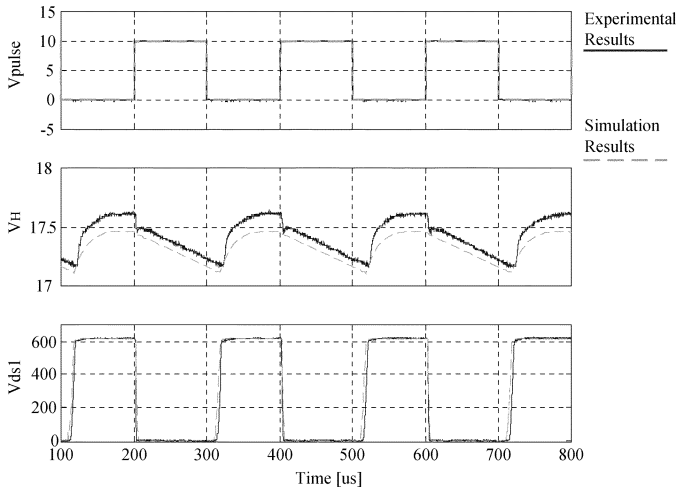

Fig. 14. Simulation and experimental results for $V_{\rm PULSE}$, V_H, and $V_{\rm DS1}$.

1200-V IGBT with a 100-A current rating at frequencies in the 10–20 kHz range [8].

The ripple voltage can be calculated from (10)

$$\Delta V_H = \frac{I_L}{C_H}\frac{\delta 1+\delta 2}{f} = \frac{0.028*(0.6)}{(10e-6*5000)} = 0.34\ \text{V}. \quad (22)$$

The sum of the charging- and boost-mode duty cycle values $(\delta_1+\delta_2)$ is assumed to be 0.6 (i.e., δ_2 =0.1) based on the selected circuit design values.

Rearranging (21), the maximum high-side output voltage $V_{\rm H,MAX}$ can be approximately calculated to be

$$\begin{aligned} V_{\rm H,MAX} &\cong V_{\rm CC} - V_{\rm D1} - V_{\rm D2} - V_{\rm D3} - \frac{C_H}{C_L}\frac{\Delta V_H}{(\delta_1+\delta_2)} \\ &= 20 - 0.8 - 0.8 - 0.2 - (1.67*0.34) \\ &= 17.6\ \text{V} \end{aligned} \quad (23)$$

where it is assumed that the $V_{\rm D1} = V_{\rm D2} = 0.8$ V and $V_{\rm D3} = 0.2$ V because D_1 and D_2 are high-voltage diodes and D_3 is a Schottky diode.

Fig. 14 shows experimental waveforms and overlaid simulation results for the input control voltage $V_{\rm PULSE}$, the high-side capacitor voltage V_H, and the switch S_1 drain-source voltage $V_{\rm DS1}$ under steady-state conditions. The measured value of the ripple voltage ΔV_H is approximately 0.4 V which is small enough to insure robust performance of the high-side gate drive.

The calculated maximum capacitor voltage $V_{\rm H,MAX}$ and ripple voltage ΔV_H values demonstrate satisfactory agreement with the measured values ($V_{\rm H,MAX-Meas} = 17.6$ V and $\Delta V_{H-Meas} = 0.45$ V). The simulated and experimental waveshapes also exhibit good agreement, although the measured V_H waveform in Fig. 14 exhibits a small sudden downward step at the beginning of the charging mode that is not predicted by the simple analysis presented above. The amplitude of this step is approximately 0.1 V, nearly equal to the difference between the calculated and measured values of ΔV_H. Investigation has revealed that this voltage step is caused by the reverse recovery current of diode D_2 when S_1 turns on. Stored charge in C_H is transferred to C_L during the D_2 reverse recovery interval, resulting in the observed voltage step. This diode reverse recovery characteristic is not been included in the simulation model, so the voltage step does not appear in the simulated V_H waveform in Fig. 14.

The value of the S_1 turn-on interval t_{21} can be measured directly from the experimental waveforms in Fig. 14 to be approximately 20 μs. Even though the duty cycle of $V_{\rm PULSE}$ (i.e., δ_1) is set at 0.5, the actual duty cycle of the C_H charging interval $(=1-\delta_1-\delta_2)$ is approximately 0.4, meaning that the t_{21} boost-mode interval reduces the charging duty cycle by approximately 20% (from 0.5 to 0.4). Reducing the value of δ_2 would cause the ripple voltage amplitude ΔV_H to decrease, but the penalty of higher losses in resistor R_3 must be considered as discussed previously in Section II. The average power dissipation in resistor R_3 is calculated to be approximately 92 mW using (20) compared to the delivered high-side output power of 476 mW.

IV. Conclusion

This paper has described a new self-boost charge pump topology for a floating high-side gate drive power supply. This new power supply circuit provides the following attractive features compared to conventional techniques:

1) robust gate drive power availability for high-side switch that eliminates phase-leg refresh switching requirements even if the high-side switch is permanently on;
2) simple charge-pump configuration requiring no high-frequency magnetic components;
3) high steady-state current supply capability for high-performance gate drives;
4) configurable to provide bipolar gate source voltages for high-side switch;
5) compatible with integrated circuit implementation.

A model for each circuit mode has been derived using piecewise-linear device models. Taken together, these models provide useful predictions of both steady-state and transient oper-

ating characteristics, as well as valuable insights regarding design considerations. Both simulation and experimental results have been presented to confirm the promising operating characteristics of the self-boost charge pump circuit. Guidelines have been presented to provide assistance with selection of circuit component values for applying this high-side power supply circuit to new applications.

REFERENCES

[1] HW floating MOS-gate drive ICs, in IR Application Note AN-978, International Rectifier Corp., El Segundo, CA.

[2] S. Storti, F. Consiglieri, and M. Paparo, "A 30 A 30 V DMOS motor controller and driver," *IEEE J. Solid-State Circuits*, vol. 23, no. 12, pp. 1394–1401, Dec. 1988.

[3] G. D. Cataldo and G. Palumbo, "Double and triple charge pump for power IC: dynamic models which take parasitic effects into account," *IEEE Trans. Circuits Syst.*, vol. 40, no. 2, pp. 92–101, Feb. 1993.

[4] R. L. Lin and F. C. Lee, "Single-power-supply-based transformerless IGBT/MOSFET gate driver with 100% high-side turn-on duty cycle operation performance using auxiliary bootstrapped charge pumper," in *Proc. IEEE Power Electronics Specialties Conf. (PESC)*, Jun. 1997, pp. 1205–1209.

[5] G. F. W. Khoo, D. R. H. Carter, and R. A. McMahon, "Analysis of a charge pump power supply with a floating voltage reference," *IEEE Trans. Circuits Syst.*, vol. 47, no. 10, pp. 1494–1501, Oct. 2000.

[6] ——, "Comparison of charge pump circuits for half-bridge inverters," *Proc. Inst. Elect. Eng.*, vol. 147, pp. 356–362, Dec. 2000.

[7] B. J. Baliga, *Power Semiconductor Devices*. Boston, MA: PWS, 1995, pp. 387–397.

[8] Agilent Technologies, "2.0 amp gate drive optocoupler with integrated desaturation detection and fault status feedback," HCPL-316J Data Sheet, 1999.

Shihong Park (S'01) received the B.S. degree in electrical engineering from Yonsei University, Seoul, Korea, in 1988, and the M.S. and Ph.D. degrees from the University of Wisconsin, Madison, in 2003 and 2004, respectively.

From 1988 to 1998, he was with Samsung Electronics, Buchen, Korea, as a Senior Power IC Design Engineer. In 2004, he was a Principal Research Engineer with Fairchild Semiconductor Korea, Buchen, Korea. In March 2005, he joined the School of Electrical, Electronics, and Computer Engineering, Dankook University, Seoul. His main research interests are integrated power electronics modules (IPEMs), power ICs and devices for automotive applications, active gate drive topology, and power converter circuit.

Thomas M. Jahns (F'93) received the S.B. and S.M., and Ph.D., degrees from the Massachusetts Institute of Technology (MIT), Cambridge, in 1974 and 1978, respectively, all in electrical engineering.

He joined the Faculty of the University of Wisconsin-Madison (UW-Madison) in 1998 as a Grainger Professor of Power Electronics and Electric Machines in the Department of Electrical and Computer Engineering. He is an Associate Director of the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). Prior to coming to UW-Madison, he worked at GE Corporate Research and Development (now GE Global Research Center), Schenectady, NY, for 15 years, where he pursued new power electronics and motor drive technology in a variety of research and management positions. His research interests include permanent magnet synchronous machines for a variety of applications ranging from high-performance machine tools to low-cost appliance drives. From 1996 to 1998, he conducted a research sabbatical at MIT, where he directed research activities in the area of advanced automotive electrical systems and accessories as co-director of an industry-sponsored automotive consortium.

Dr. Jahns received the William E. Newell Award from the IEEE Power Electronics Society (PELS) in 1999. He has been recognized as a Distinguished Lecturer by the IEEE Industry Applications Society (IAS) from 1994 to 1995 and by IEEE-PELS from 1998 to 1999. He has served as President of PELS (1995–1996) and as a Member of the IAS Executive Board from 1992 to 2001. From 2002 to 2003, he was the Division II Director on the IEEE Board of Directors.