Ultrahigh-Performance 8-GHz SiGe Power HBT

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***Abstract*—This letter has demonstrated the state-of-the-art SiGe power heterojunction bipolar transistors (HBTs) operating at 8 GHz. In a common–base configuration, a continuous wave output power of 27.72 dBm with a concurrent power gain of 12.19 dB was measured at a peak power-added efficiency of 60.6% from a single SiGe HBT with a 3-μm emitter finger stripe width and a 1340 μm^2 total emitter area. The highest power-performance figure of merit (FOM) of 3.8×10^5 mW · GHz^2 achieved from the device was resulted from using an optimized SiGe heterostructure and a compact device layout, which is made possible with a heavily doped base region.**

***Index Terms*—Common–base (CB), heterojunction bipolar transistors (HBTs), SiGe, X-band.**

I. Introduction

ALONG WITH the development of high-speed SiGe heterojunction bipolar transistors (HBTs), power SiGe HBTs were also developed in recent years [1]–[5]. Due to the power gain degradation with the increase of operation frequencies (-10 dB/dec for maximum stable power gain (MSG) and at least -20 dB/decade for maximum available power gain (MAG)) and with the increase of a device size (increased parasitics and thermal effects), degraded power gain, and power-added efficiencies (PAEs) are inevitable when large-area devices are operated at higher frequencies. Nevertheless, high-power gain and high-PAE values are always desired for the implementations of power SiGe HBTs in power amplifiers. Unfortunately, as of today, high-PAE values ($> 50\%$) have never been achieved for single SiGe power HBTs that are operated at X-band and beyond with an output power of over 0.5 W. While SiGe HBTs have shown the promise for RF and microwave applications with a higher level integration than the III–V counterparts, it is imperative to develop high-frequency (C- and X-bands) power SiGe HBTs that exhibit a higher power gain and a higher efficiency to make these devices fulfill the requirements of power amplification in these frequency ranges. In this letter, we report the design and characterization of the state-of-the-art 8-GHz SiGe power HBTs that exhibit more than five times improvement on the overall power performance over the previously reported best ones [5].

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II. Device Design and Fabrication

It is recently shown [6] that by reducing the value of base resistance (R_B), the MAG of both common–emitter (CE) and common–base (CB) SiGe HBTs and the MSG of CB SiGe HBTs can be improved. It is also shown [6] that by reducing the base–collector junction capacitance (C_{BC}), the power gain ($G_{\max}$) of SiGe HBTs under both configurations can be improved. Besides these intrinsic device parameters that affect the power gain of SiGe HBTs, the power performance of large-area devices can be further improved with the reduction of parasitics.

Conventionally, the downscaling of emitter stripe width has been used to reduce the base resistance of Si-based bipolar junction transistors (BJTs). The underlying reason is that the lateral downscaling of the emitter stripes can reduce the emitter current crowding effect [7]. SiGe HBTs with doping profiles similar to that of Si BJTs usually have high pinch-base resistance values due to the use of relatively low-base doping concentrations (N_B). As a result, shrinking the emitter stripe width is an effective measure to improve R_B in these devices. The conventional downscaling approach has been proven to be successful and has been widely used in commercial SiGe HBTs.

An alternative approach to minimizing the emitter current crowding effect in SiGe HBTs is to increase N_B. With a high N_B, the pinch-base sheet resistance of the devices will be reduced. Consequently, wider emitter stripes can be used without causing a severe emitter current crowding effect during a device operation. The viability of using wider emitter stripes in SiGe power HBTs with a high N_B enables less number of emitter stripes to be needed than using narrower emitter stripes in order to achieve the same RF power level. With the reduction of the number of the emitter stripes, the number of base and collector stripes will also be accordingly reduced. As a result, a higher power density can be realized per unit chip area. Of more importance, the reduction of base contact number results in a smaller C_{BC}, since C_{BC} is directly proportional to the emitter and base stripe area in mesa-type SiGe HBTs. Due to the reduction of C_{BC}, $G_{\max}$ [6] will thus be improved. Furthermore, a compact size of the power devices that can be realized using less numbers of emitter, base, and collector stripes allows shorter interconnect metal to be used. Therefore, less parasitics from the interconnects will be introduced into the devices and less power gain degradation due to the parasitics can be achieved.

In the recent study [6], it is shown that employing a heavily doped base region to substantially reduce base-resistance values can make $G_{\max}$ of CB SiGe HBTs much high than that of CE HBTs. Using such a base optimization strategy and CB configuration, the highest power-performance results have

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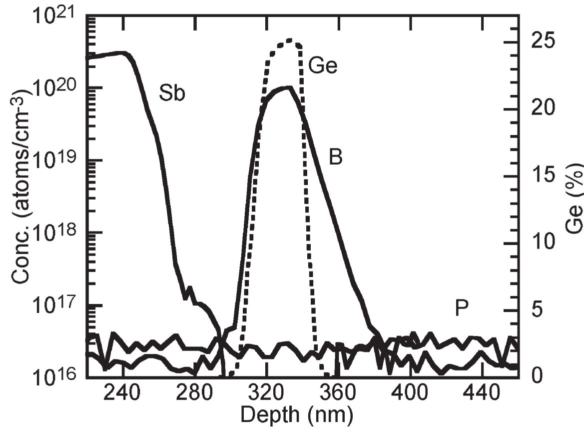

Fig. 1. Measured SIMS profile of SiGe heterostructures used for a device fabrication. A heavy base doping concentration (1×10^{20} cm^{-3}) is used in the heterostructure to reduce the pinch-base resistance of SiGe HBTs.

been achieved previously for SiGe power HBTs operated at X-band [5]. Apparently, in order to achieve a higher power performance, it is necessary to further increase the N_B of SiGe HBTs and, furthermore, using CB configuration to achieve the higher power performance than CE is still justified.

In the heterostructure design of the SiGe power HBTs, a high N_B of 1×10^{20} cm^{-3} with 30-nm SiGe (25% Ge) base thickness was used to reduce the base sheet resistance ($R_{\rm sh}$). The measured secondary ion mass spectroscopy (SIMS) profile is shown in Fig. 1. Because of the high N_B, a record low $R_{\rm sh}$ of only 565 $\Omega/\Box$ (measured from TLM patterns) was obtained. Such an extremely low $R_{\rm sh}$ value allows wide ($W_E = 3$ μm) emitter stripes to be employed in the device layout. These emitter stripes (length $L_E = 30$ μm) were formed in subcell structures with two emitter stripes in each subcell surrounded by base stripes of 2 μm. To reduce the interconnect metal resistance, a 32-μm-wide base-interconnect metal (gold) layer, with 1.5-μm thickness, was designed. The SiGe HBTs were fabricated using a standard double-mesa process [8]. The photomicrograph of a fabricated SiGe HBT with 14 emitter finger stripes and total emitter area (A_E) of 1340 μm^2 is shown in Fig. 2(a). For comparison, the photomicrograph of a SiGe HBT with the same A_E but $W_E = 2$ μm is shown in Fig. 2(b). It can be easily calculated that, by using wider emitter stripes ($W_E = 3$ μm instead of 2 μm), the base mesa area (hence the $C_{\rm BC}$) is reduced by about 25%. In addition, the total chip area of the device was reduced from 226×64 μm^2 [Fig. 2(b)] to 160×64 μm^2 [Fig. 2(a)]. Due to the reduction of the device layout span, the length of the base-interconnect metal (running on top of the subcells) is shortened. Hence, the parasitic resistance of the interconnect is reduced by about 30% solely from the length reduction.

III. Device Performance

A dc, small-signal S-parameters and a large-signal power performance of CB SiGe HBTs with 3-μm emitter stripes and a 1340-μm^2 emitter area were characterized. Due to the employment of a thick (0.5 μm) and lightly doped (2.5×10^{16} cm^{-3}) collector epilayer, high breakdown voltages $\rm BV_{CEO}$ of 8.5 V and $\rm BV_{CBO}$ of 14 V were obtained. Although, 3-μm emitter stripes and a "compact" device layout were used, no current collapse was observed from dc current–voltage (I–V) measurements (dc current gain β is 22 in CE configuration). The small-signal S-parameters of the devices were characterized using an Agilent E8364A network analyzer. Fig. 3 shows the $G_{\max}$ (MSG/MAG) values versus frequency of the devices. At 8 GHz, the MSG is measured to be 15.5 dB.

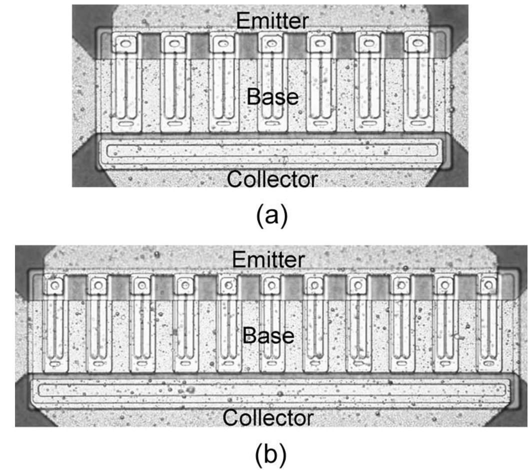

Fig. 2. SEM photomicrographs of fabricated mesa-type multifinger CB SiGe HBTs. Both devices have a total emitter area $A_E = 1340$ μm^2. (a) $W_E = 3$ μm and total 14 emitter stripes and (b) $W_E = 2$ μm and total 22 emitter stripes. Stripe length $L_E = 30$ μm for both devices.

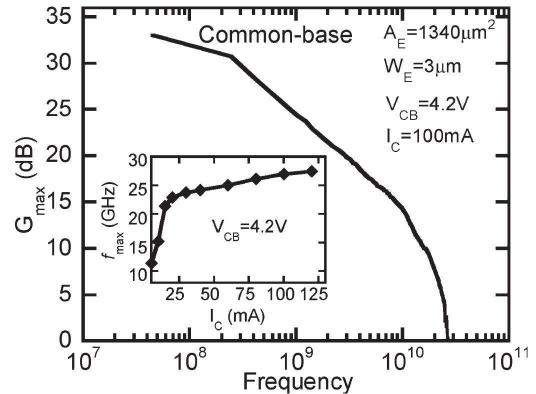

Fig. 3. Measured $G_{\max}$ (MSG/MAG) versus frequency and $f_{\max}$ versus I_C (inset) for a power SiGe HBT ($W_E = 3$ μm and $A_E = 1340$ μm^2) under the CB configuration. The $G_{\max}$ at 8 GHz is 15.5 dB.

The power-performance characteristics of the CB SiGe HBT were characterized at 8 GHz using a Focus Microwaves CCMT1816 source/load pull system. Biased at class AB with $V_{\rm CB} = 5$ V, $V_{\rm BE} = 0.69$ V, the device was operated under continuous wave mode and both input and output were matched for a maximum output power. The measurements were carried out on wafer (540-μm thick) and no special heat dissipation technique was employed. Fig. 4 shows the measured output power ($P_{\rm out}$), power gain, PAE, and collector current (I_C) as a function of input power ($P_{\rm in}$), along with the calculated FOM. The measured peak PAE is 60.6% ($P_{\rm dc} = 917$ mW), which is much higher than any reported values for SiGe power HBTs operated at X-band and beyond. The output power and power gain are 27.72 dBm and 12.2 dB, respectively, at the peak PAE point. The saturated output power is 28 dBm. The

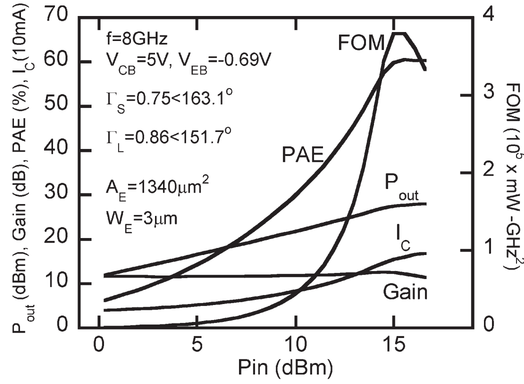

Fig. 4. Measured power performance and calculated FOM of a CB SiGe HBT ($W_E = 3$ μm and $A_E = 1340$ μm^2) biased under class AB operation. An output power of 27.72 dBm and concurrent power gain of 12.2 dB were obtained at peak PAE of 60.6%. The calculated peak FOM is 3.8×10^5 mW $\cdot$ GHz^2.

TABLE I
PERFORMANCE COMPARISON AMONG REPORTED SiGe POWER HBTs

Freq. (GHz)	P_{out} (dBm)	Gain (dB)	PAE (%)	FOM (mW·GHz^2)	W_E (μm)	Ref.
1.9	32.4	12.3	67	7.6×10^4	0.9	[3]
5.35	24.7	13.6	33	6.4×10^4	0.5	[2]
8.4	26.7	8.3	31	7.0×10^4	2	[5]
12.6	21.6	7.4	23	2.9×10^4	1.4	[1]
18	24.7	3.7	11	2.5×10^4	2	[4]
8.0	27.7	12.2	61	3.8×10^5	3	This work

high PAE achieved from the device lowers the heating power $[P_{\text{heat}} = P_{\text{dc}} \cdot \text{(1-PAE)}]$ to 361 mW or 0.27 mW/μm^2. The low-heating power density improves the thermal stability of the device without using external ballasting resistors. The calculated power-performance FOM ($\text{FOM} = P_{\text{out}} \cdot G \cdot f^2 \cdot \text{PAE}$) [9] of the device is 3.8×10^5 mW $\cdot$ GHz^2. To our knowledge, this is the highest FOM value achieved among all reported single SiGe power HBTs operated at any frequencies. A performance comparison among all published power SiGe HBTs is summarized in Table I with the emitter stripe widths listed for reference.

The superior power-performance results demonstrated in this letter are ascribed to the reduced R_B, C_{BC}, and parasitics in the device. The reductions of these parameter values are made possible by using a very high N_B that provides a very low R_{sh}. The low R_{sh} value relaxes the emitter current crowding effect and thus permits wide emitter stripes and a compact device layout to be used. Both C_{BC} and interconnect parasitics are reduced in the compact layout. Furthermore, the wider and thicker interconnect metal than that used in the previous state-of-the-art SiGe HBTs [5] further reduces the parasitic resistance and hence increases the power gain and PAE of the device.

IV. CONCLUSION

The state-of-the-art SiGe power HBT has been developed with P_{out} of 27.72 dBm and concurrent power gain of 12.2 dB at peak PAE of 60.6% measured at 8 GHz. The highest FOM of 3.8×10^5 mW $\cdot$ GHz^2 achieved from the device was resulted from using a heavily doped base region (1×10^{20} cm^{-3}) to obtain an ultralow-base sheet resistance (565 $\Omega/\square$), which permits a compact device layout to be used with reduced base-collector junction capacitance and interconnect parasitics.

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