A Current Source PWM Inverter With Actively Commutated SCRs

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***Abstract*—Conventional SCR based current source inverters suffer from poor waveform quality due to six step switching. Pulse width modulated current source inverters typically require gate turn off devices with reverse voltage blocking capability which have limited their application. In this paper, a new pulse width modulated current source inverter topology using one gate turn off switch and six SCRs is presented. The converter uses active commutation to realize pulse width modulation in a conventional SCR based current source inverter. Modulation techniques for the proposed inverter, simulation and experimental results are described in the paper. This topology is suitable for high performance, high power applications.**

***Index Terms*—Active commutation, current source inverters, hybrid topology, pulse width modulation, SCR.**

I. Introduction

With the availability of modern gate-turn-off switching devices at increasing power levels and the introduction of advanced multilevel power converter topologies, the classical current source inverter (CSI) topology has been virtually replaced by the voltage source inverter (VSI), even in applications up to several MW. However, SCR based CSI systems are still being used for very high power synchronous motor drives and utility power systems due to various performance advantages. CSI topologies have certain performance advantages in terms of ruggedness and their ability to feed capacitive and low impedance loads with ease. As high power permanent magnet motors with extremely low armature winding inductance are becoming more common and the electrolytic capacitor of a VSI becoming notorious as the largest and least reliable among inverter components, a renewed interest in CSI systems may be expected to follow.

The classical CSI based on SCRs (Fig. 1) has several disadvantages. They simply stem from the fact that SCRs cannot be turned off from the gate. Hence, their operation has been typically limited to six-step switching and application to active loads capable of operation at leading power factor [1]. Six-step switching leads to a large amount of harmonics in the load voltage and current. Hence, they have been naturally bucked by the trend of increasing demands of performance. Furthermore, they are not well suited to drive induction motors, which must operate at a lagging power factor. These reasons have generally impeded their widespread application. Replacement of the SCR with a GTO device would allow turn-off capability and result in the extension of operation to loads with wider power factor and even pulse width modulation (PWM) capability [2]. However, due the limited switching speeds of GTOs this approach has seen limited application. More commonly, GTO devices have been adapted to operate in multilevel VSI systems [3]. Switching throws in a CSI realized using bi-directional voltage blocking and unidirectional current carrying devices have been well known [4]. Fig. 2 illustrates such a realization using insulated gate bipolar transistor (IGBT) devices in series with diodes. This topology is plagued with low efficiency due to current flow through the series connection of two semiconductors per throw.

The objective of this paper is to explore the topological design space of current source inverters to enable them with pulse width modulation to synthesize high quality ac waveforms, while retaining the use of SCRs to realize the throws of the inverter bridge [5]. The paper proposes a succinct but strategic placement of one gate-turn-off device such as an IGBT on the dc side of the CSI to realize PWM capability, and accommodation of loads with a wider range of power factor.

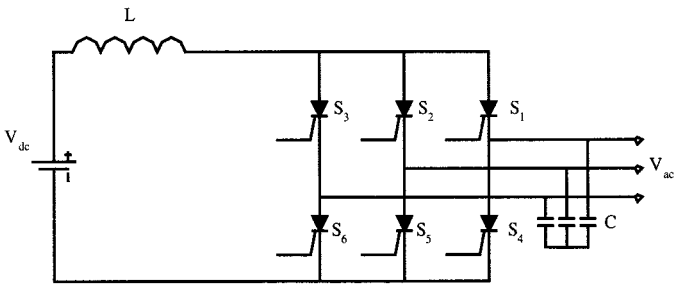

Fig. 1. Schematic of a classical SCR based CSI.

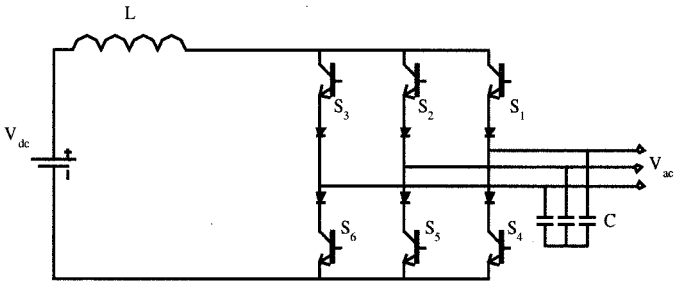

Fig. 2. Schematic of a CSI using IGBTs and series diodes.

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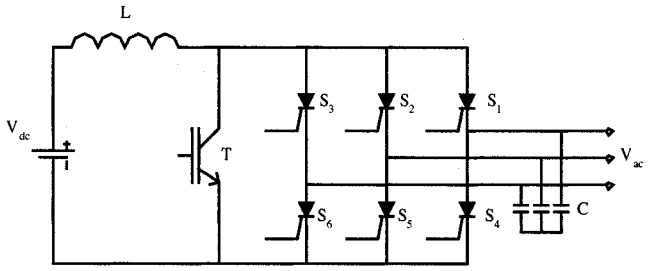

Fig. 3. Schematic of the proposed boost inverter topology.

The topology and its operation are explained in Section II. The principles and limitations of active commutation of the SCR bridge using a dc side switch are described and illustrated using experimental waveforms. In Section III, the analysis of converter operation using averaged switching functions is presented. Transfer properties relating the input and output variables with the duty ratio functions are developed. Section IV presents the converter control algorithm and modulation schemes for the proposed converter. Computer simulation results verifying the operation of the converter and modulation algorithms are presented in Section V, followed by a concluding discussion in the final section.

II. SCR PWM Boost Inverter

The schematic of the power circuit of the PWM current source inverter using actively commutated SCRs is illustrated in Fig. 3. As may be observed from the figure, the topology is derived by the addition of a gate-controlled switch, T (an IGBT, as shown in the figure) across the bridge inverter on the dc side. Using T, the SCRs can be actively commutated, thus permitting pulse width modulation of the switch throws.

A. Active Commutation

Fig. 4(a)–(c) illustrate the current flow path during a typical operating sequence of the inverter. When T is off, the dc side inductor current flows through one SCR in the upper half, i.e., S_1, S_2, or S_3 out to the load and returns through one SCR in the lower half, i.e., S_4, S_5, or S_6. During this time, the remaining four SCRs are off. In Fig. 4(a), the inductor current flows through S_1 to the load and back through S_5. If at some instant, if T is turned on, the inductor current is diverted away from the inverter bridge and the SCR currents are driven to zero. Furthermore, for typical unity power factor loads, a reverse voltage from the load is also imposed upon them, thus ensuring turn-off of the bridge [6]. As T actively provides a path for the recovery current in the SCRs, this process may be termed "Active Load Commutation." This condition is illustrated in Fig. 4(b). During this period, with the T maintained in its on-state, additional energy is stored in the dc inductor, which also results in a boost function for the output voltage. After this commutation interval, a new set of two SCRs, say S_3 and S_4 can be gated on with zero voltage across them. When the T is turned off, the dc current flows through the two newly chosen SCRs to the load, and the inverter is in its new modulation state as illustrated in Fig. 4(c).

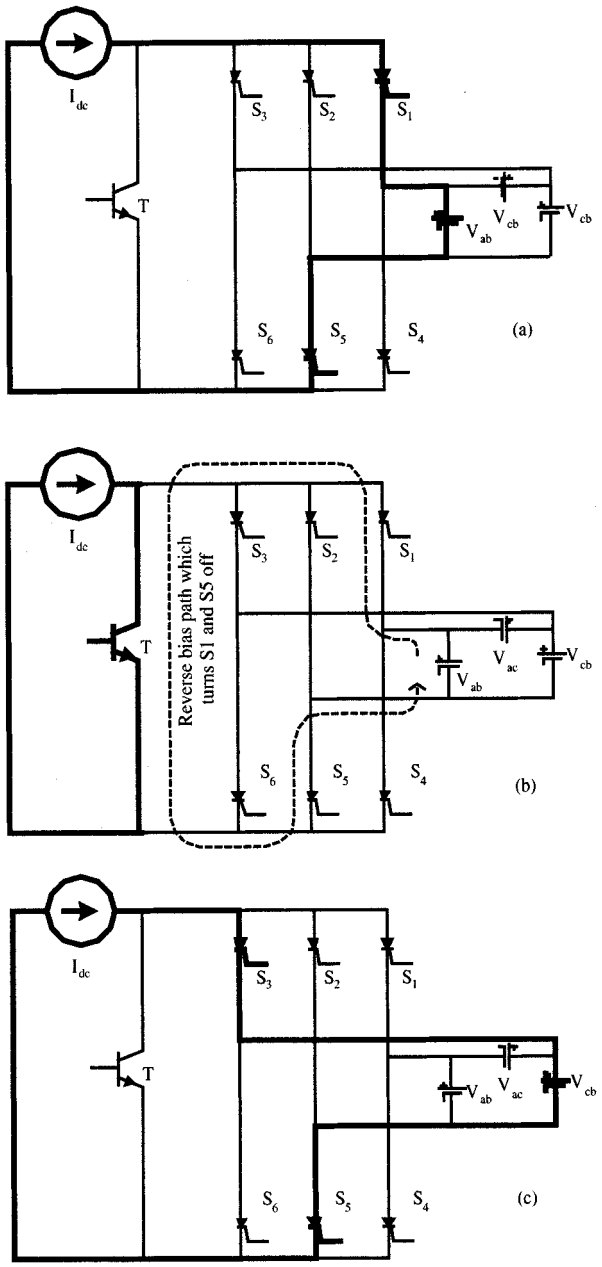

Fig. 4. Schematic of current flow during typical switching states and commutation modes in the proposed converter.

If the active commutation of the SCRs can be done at a high enough frequency (up to 5 kHz), the size of the dc bus inductor and the output filter capacitors are reduced and the harmonic content of the load current can be well controlled.

B. Test Circuit

It may be easily seen that the key to successful operation of the proposed approach is the active commutation of the SCRs. In order to verify the operation of this commutation mode, an experimental test circuit was built (Fig. 5). The test circuit consists of a boost converter employing two SCRs feeding two loads in place of the single rectifier diode. The two SCRs are alternatively gated on during every other switching cycle of the IGBT turn off period, so that one of them is in the blocking state while

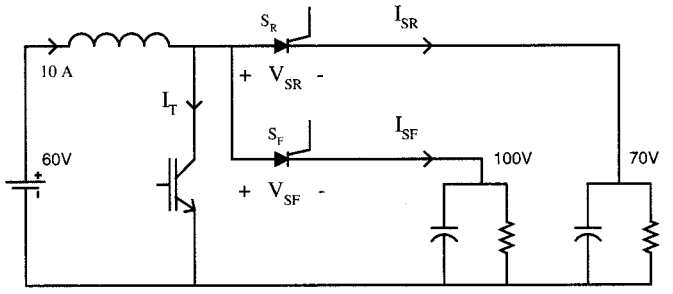

Fig. 5. Schematic of the test circuit used for characterizing active commutation of SCR.

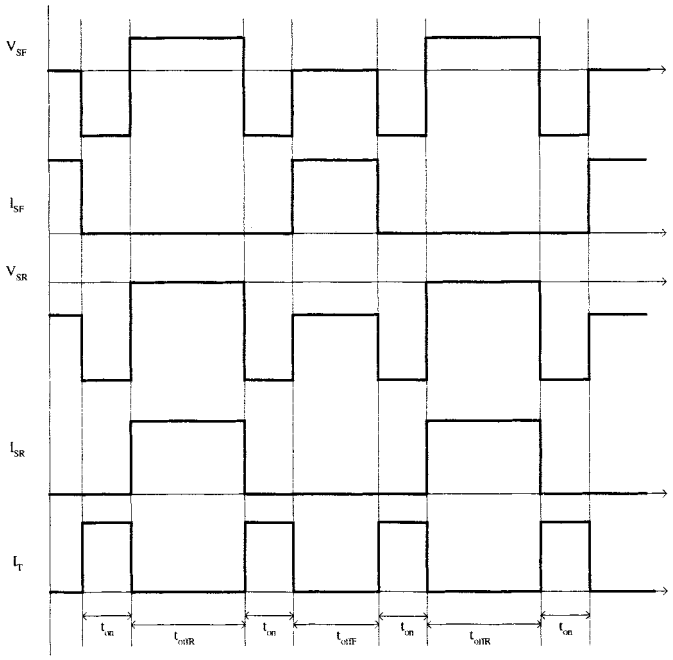

Fig. 6. Ideal test circuit waveforms under different operating intervals during a switching period.

the other one is in the conducting state. Under typical operating conditions, both the SCRs block a negative voltage during the IGBT on-state. However, one of the SCRs (S_R) blocks reverse voltage during the IGBT off-state and the other SCR (S_F) blocks forward voltage during IGBT off state. Thus, the SCR switching waveforms in the test circuit would be identical to those seen in the inverter. During the tests, the corresponding incoming SCRs were always gated on before the IGBT gate was turned off. This ensures that a continuous path for the inductor current is readily present under all conditions. Typical idealized switching waveforms that would be obtained from the test circuit are illustrated in Fig. 6. During the intervals $(t_{\rm on})$, when the IGBT is on, both the SCRs block reverse voltage. When the IGBT is off, during $t_{{\rm off}R}$, S_R is conducting and the voltage across it is zero, while the voltage across S_F is positive. During $t_{{\rm off}F}$, S_F is conducting and the voltage across it is zero, while the voltage across S_F is negative (see Fig. 7).

Waveforms from the actual test circuit are shown in Fig. 8. The waveforms indicate circuit operation as intended, except for the deviations during switching transients.

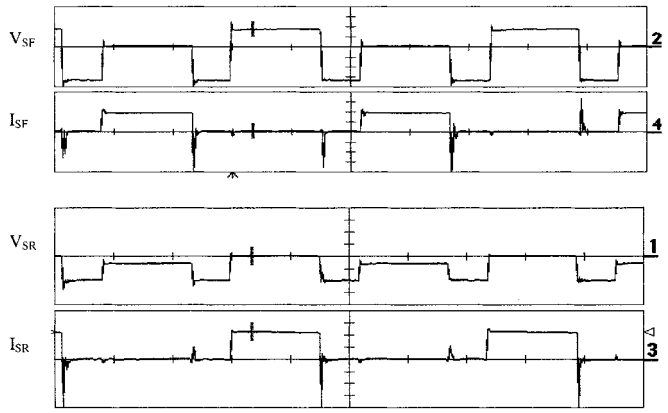

Fig. 7. SCR voltage (50 V/div) and current (5 A/div) waveforms (200 μs/div) under active commutation obtained using the experimental test circuit.

During SCR turn-off, the IGBT is initially open and one of the SCRs is carrying the inductor current. When the IGBT is turned on the current through the conducting SCR is picked up rapidly by the device. While the current in the IGBT is rising, the parasitic inductance of the commutation loop absorbs the voltage and hence the IGBT voltage is low. When the IGBT current reaches the inductor current, the SCR reverse recovery current flows through the IGBT, until the SCR finally turns off. The rapid decay of the SCR current after the recovery results in a substantial voltage being developed across the commutation loop inductance and results in a reverse voltage spike across the SCR, as may be seen in the figure. Through judicious use of controlled rate of turn-on of the IGBT current, addition of device clamps, snubbers and low inductance bus planes, the reverse recovery loss and associated voltage spikes can be minimized.

When the IGBT is turned off after the SCR has been latched on, the rapidly decaying IGBT current is transferred to the SCR. Effects of forward recovery are seen in the SCR voltage at turn on. The IGBT turn off rate has to be low enough to keep the SCR within its di/dt limits. Bus planes, snubbers and clamps can be used to alleviate the turn off voltage stresses on the IGBT.

It should be noted that the SCRs would have to be maintained off for a minimum amount of time before being turned on again to prevent commutation failures. However, preliminary investigations indicate that with the use of inverter grade SCRs and IGBTs, switching frequencies in the range of 3 to 5 kHz are realizable.

III. Converter Steady State Modeling

In this section, an averaged fundamental component model of the PWM CSI and the various duty ratio modulation functions are developed. The six SCRs and the boost switch modulate the dc link current into the output phases. The switching functions for these devices are designed so that the fundamental components of the phase currents approximate balanced three phase sinusoids [7].

A. Fundamental Component Model

A simplified equivalent circuit of the boost-derived current source inverter with complete control capability can be repre-

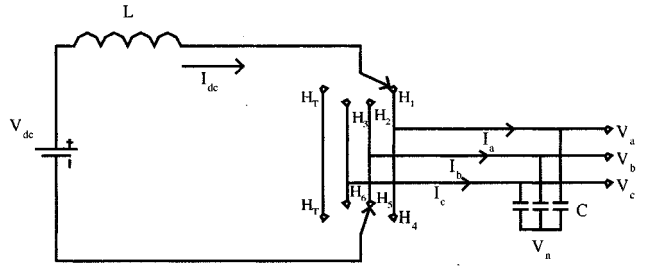

Fig. 8. Ideal switch equivalent circuit of the PWM CSI converter.

sented by two single pole quadruple throw switches as illustrated in Fig. 8. Throws 1 through 7 represents the corresponding SCRs S_1 through S_6 and throw T represents the controllable switch, T.

Let H_1-H_6 be the switching functions of the six SCR throws, and H_T be the switching function of T. Continuity of the inductor current can be explicitly constrained using the following relationships:

$$H_1 + H_2 + H_3 + H_T = 1 \tag{1}$$
$$H_4 + H_5 + H_6 + H_T = 1. \tag{2}$$

With the switching functions defined as above, the three phase pole currents $(I_a - I_c)$ can be represented in terms of the inductor current $(I_{\rm dc})$ as

$$\begin{aligned} I_a &= (H_1 - H_4) I_{\rm dc} \\ I_b &= (H_2 - H_5) I_{\rm dc} \\ I_c &= (H_3 - H_6) I_{\rm dc}. \end{aligned} \tag{3}$$

If the average values of the switching functions $H_1 - H_6$ and H_T are given by their duty ratios $D_1 - D_6$ and D_T respectively, (3) can be represented as

$$\begin{aligned} I_a &= (D_1 - D_4) I_{\rm dc} \\ I_b &= (D_2 - D_5) I_{\rm dc} \\ I_c &= (D_3 - D_6) I_{\rm dc}. \end{aligned} \tag{4}$$

If effective duty ratios D_a, D_b and D_c are defined as $D_1 - D_4$, $D_2 - D_5$ and $D_3 - D_6$ respectively, the three phase currents may be derived to be

$$\begin{aligned} I_a &= (D_a) I_{\rm dc} \\ I_b &= (D_b) I_{\rm dc} \\ I_c &= (D_c) I_{\rm dc}. \end{aligned} \tag{5}$$

In order to synthesize sinusoidal phase currents, the effective duty ratios D_a, D_b and D_c may be chosen to be a set of balanced sinusoidal functions of frequency f, with an amplitude D_m. In that case, the phase currents become

$$\begin{aligned} I_a &= I_{\rm dc} D_m \cos(2\pi f t) \\ I_b &= I_{\rm dc} D_m \cos(2\pi f t - 120^\circ) \\ I_c &= I_{\rm dc} D_m \cos(2\pi f t + 120^\circ) \end{aligned} \tag{6}$$

which may be represented as three phasors, $I_o\angle 0$, $I_o\angle -120^\circ$ and $I_o\angle +120^\circ$.

For a balanced three phase linear load, the output line to neutral voltage phasors V_a, V_b and V_c can be represented as $V_o\angle\phi$, $V_o\angle(\phi - 120^\circ)$ and $V_o\angle(\phi + 120^\circ)$, respectively. The instantaneous output power $P_{\rm out}$ is given by

$$P_{\rm out} = 3 V_o I_o \cos(\phi). \tag{7}$$

This is equal to the instantaneous power $P_{\rm dc}$ drawn from the dc source $V_{\rm dc}$, which can be expressed as

$$P_{\rm dc} = V_{\rm dc} I_{\rm dc}. \tag{8}$$

Equating (7) and (8), a relationship between effective value of line to neutral output voltage (V_o), power factor $(\cos\phi)$, dc bus voltage $(V_{\rm dc})$, and the maximum value of the effective duty ratio (D_m) can be determined to be

$$V_o = \frac{\sqrt{2}}{3} \frac{V_{\rm dc}}{\cos\phi} \frac{1}{D_m}. \tag{9}$$

Thus, for a given power factor load, increasing the maximum effective duty ratio (D_m) leads to a drop in the output voltage.

B. Modulation Functions

The effective duty cycle D_a, D_b, D_c can be decomposed into average SCR duty cycles $D_1 - D_6$ as follows

$$\begin{aligned} D_1 &= D_a u(D_a) \\ D_2 &= D_b u(D_b) \\ D_3 &= D_c u(D_c) \\ D_4 &= -D_a u(-D_a) \\ D_5 &= -D_b u(-D_b) \\ D_6 &= -D_c u(-D_c) \end{aligned} \tag{10}$$

where $u(.)$ is the unit step function. Furthermore, the average duty ratio D_T of the dc side switch is given by

$$D_T = 1 - (D_1 + D_2 + D_3). \tag{11}$$

Fig. 9 illustrates the three phase currents and the corresponding duty ratios as functions of time. From the figure, it can be seen that the duty ratio of the boost switch (D_T) is the complement of the maximum value of the various duty ratios $D_1 - D_6$

$$D_T = 1 - \mathrm{Max}(D_1 \ldots D_6). \tag{12}$$

Moreover, under sinusoidal modulation as shown in Fig. 9, the average value of D_T can be determined to be

$$D_{\rm Tavg} = 1 - \frac{3}{\pi} D_m. \tag{13}$$

Using (13) and (9)

$$V_o = \frac{\sqrt{2}}{\pi} \frac{V_{\rm dc}}{\cos\phi} \left[\frac{1}{1 - D_{\rm Tavg}} \right]. \tag{14}$$

The dc–dc boost converter's bearing the topological lineage of the PWM CSI is elucidated by this relationship.

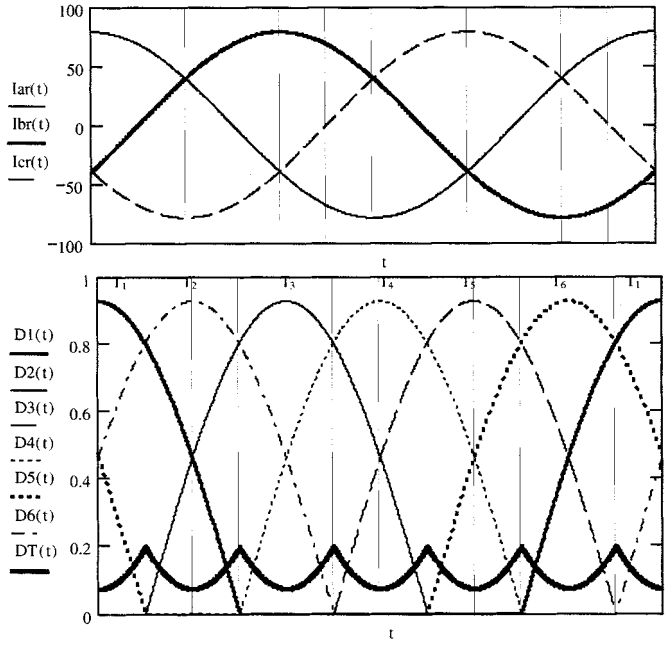

Fig. 9. Waveforms of three phase current references and switch states for the boost inverter.

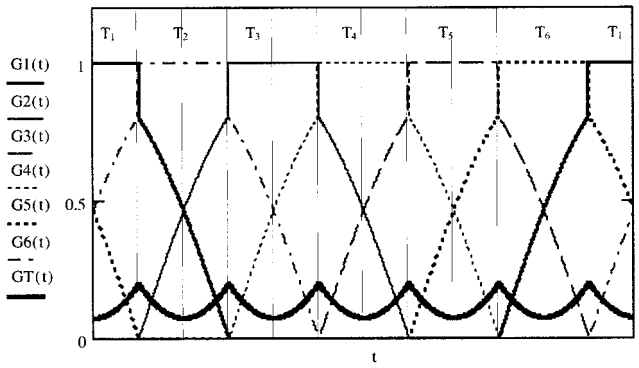

Fig. 10. Modified reference waveforms fed to sine triangle modulator.

IV. Realization of the Modulator

The pulse width modulator forms the innermost loop of the PWM CSI [8]. The modulator accepts balanced three phase sinusoidal output current commands and generates switch states for the six SCRs and the boost IGBT in an open loop manner. CSI modulator operation is easier understood if the fundamental cycle is split into six 60° increments $(T_1 - T_6)$ as shown in Fig. 9. Symmetry of the three phase waveforms permits the modulation technique to be developed for any 60° segment, and transposed accordingly.

When the reference is within a 60° band centered at its peak, the corresponding SCR is maintained on through out the interval. During the 60° interval that a given SCR is held on, the complementary SCR of the same phase has to be gated off to allow the inductor current to flow out to the load. Furthermore, at any given instant, only one of the high side SCRs S_1, S_2, or S_3 and one of the low side SCRs S_4, S_5, S_6 can be turned on to avoid output line to line shorts. Hence, it is clear that once the SCR that is to be maintained on during a given 60° has been identified, it completely dictates the three other SCRs in the bridge that have to be off. The two remaining SCRs are now modulated to achieve the desired switching function.

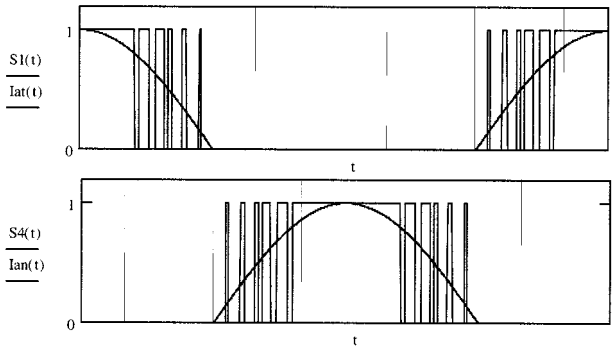

Fig. 11. Gate drive waveforms for S_1 and S_4 and a phase positive and negative reference currents.

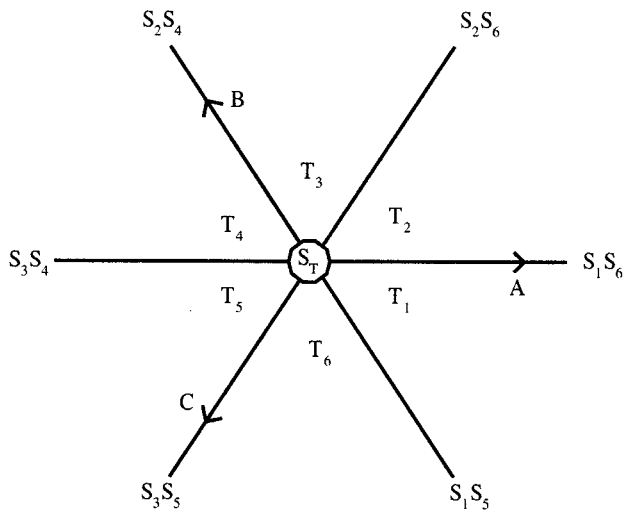

Fig. 12. Phase plane illustration of the switching states of the PWM CSI.

For example, S_1 is maintained on during the interval T_1, S_4 is maintained on during the interval T_4. During T_1, when S_1 is on, S_2, S_3, and S_4 are held off; and S_5 and S_6 are modulated to achieve the desired switching function. By saturating the sine-triangle modulator circuit appropriately during each 60° segment, the corresponding SCR can be held on. This modification to the sinusoidal references is shown in Fig. 10. These modified duty ratios are converted into gate drive signals using a conventional sine-triangle comparison technique. The gate drive commands for S_1 and S_4 obtained using this approach for the A phase are illustrated in Fig. 11.

The switching states of the CSI are summarized in Fig. 12. During any operating segment, the system chooses the three switching states that form the vertices thereof. For instance, during the segment T_3, the switching states chosen are S_2S_4, S_2S_6 and the S_T state. Every transition from S_2S_4 to S_2S_6 and vice-versa is forced to go through the S_T state. This strategy ensures successful active commutation of S_4 and S_6.

The controlled switch T is turned on during the zero state. If at least one of the high side SCRs S_1, S_2, S_3 and at least one of the low side SCRs S_3, S_4, S_5 is on, T is turned off. Otherwise, T is turned on to provide a path for the dc inductor current.

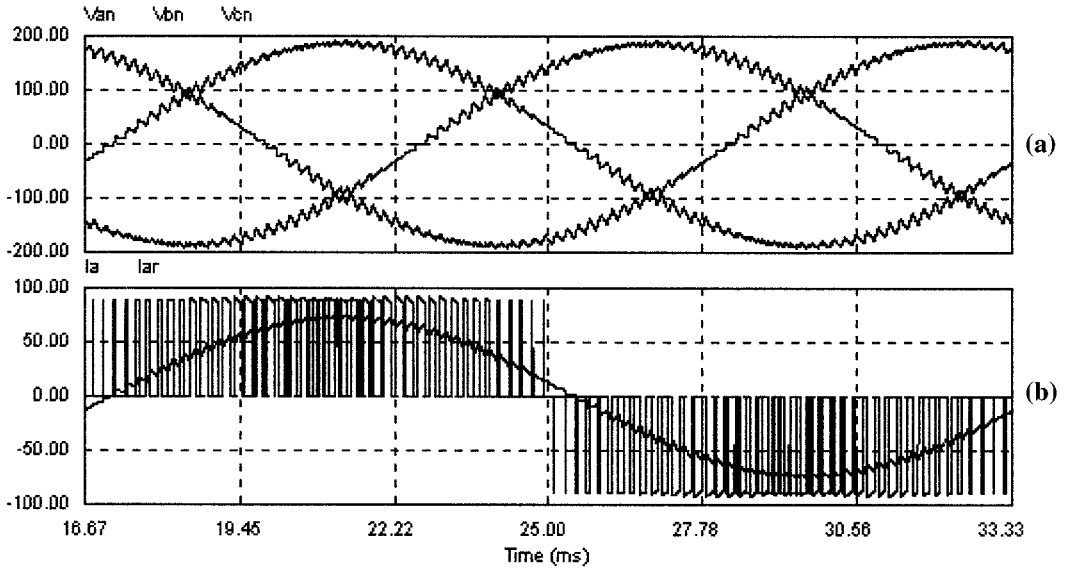

Fig. 13. Inverter output waveforms, operating at $D_m = 0.83$: (a) three phase output line-neutral voltages (V_{an}, V_{bn}, V_{cn}) and (b) phase A pole current and sinusoidal load current (I_a, I_ar).

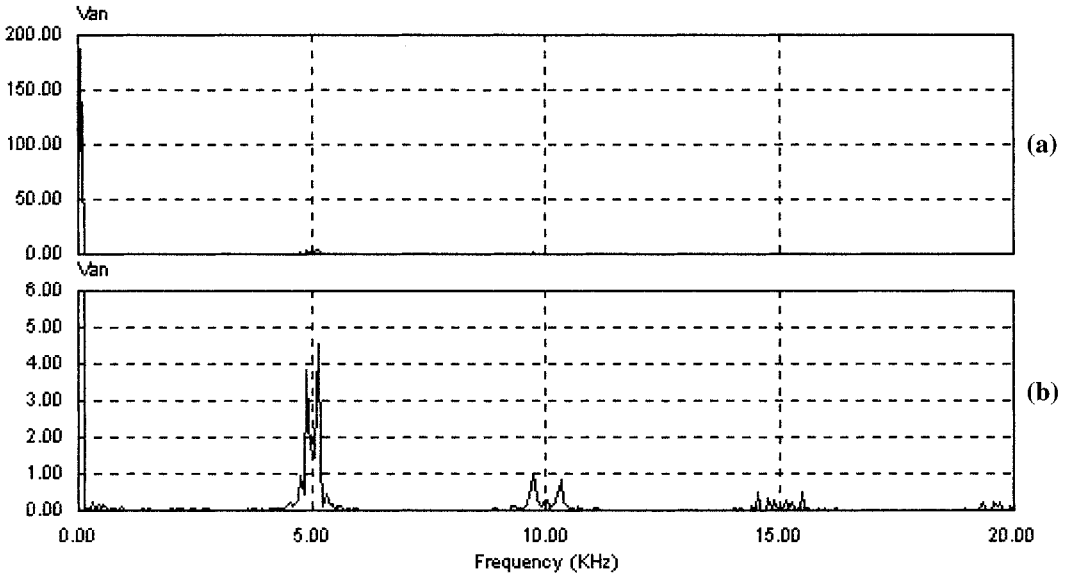

Fig. 14. (a) Spectrum of the V_{an} with $D_m = 0.83$ and (b) magnified view.

V. Simulation and Experimental Results

Digital computer simulation model was developed to verify the operation of the proposed converter and modulation schemes. The simulations were performed on an inverter with a 230 V dc bus, a 2 mH dc inductor and a 180 μF output filter capacitor with a resistive load of 2.5 Ω. The carrier frequency was chosen to be 5 kHz. The results confirm the technique of active SCR commutation and the operation of the modulator.

Fig. 13 illustrates the simulation waveforms for the inverter generating 230 V line-line while delivering 20 kW. Fig. 13(a) shows the traces of three phase output voltages, which were found to have a THD of 3.5%. The voltage ripple corresponding at the carrier frequency is evident and can be further reduced by increasing the size of filter capacitor, if deemed necessary. Fig. 13(b) shows the A phase pole current and load current. The pole current waveform verifies that the modulator produces adjacent state switching while conforming to the pulse polarity consistency rule [9]. The output voltage spectrum is presented in Fig. 14(a), while a magnified view of the carrier frequency harmonic components is highlighted in Fig. 14(b). The spectrum confirms the absence of low frequency harmonics and the undesired spectral content being limited to the sidebands of switching frequency harmonics, which may be filtered easily.

A laboratory prototype three phase inverter was built using inverter grade SCRs and an IGBTs, with a switching frequency of 5 kHz. The converter was operated in an open loop fashion to generate a 60 Hz output, feeding a resistive load. The traces of modulated current, load current and three phase output voltages are shown in Fig. 15. Successful operation of the active commutation strategy in synthesizing pulse width modulated output waveforms is readily evident from Fig. 6.

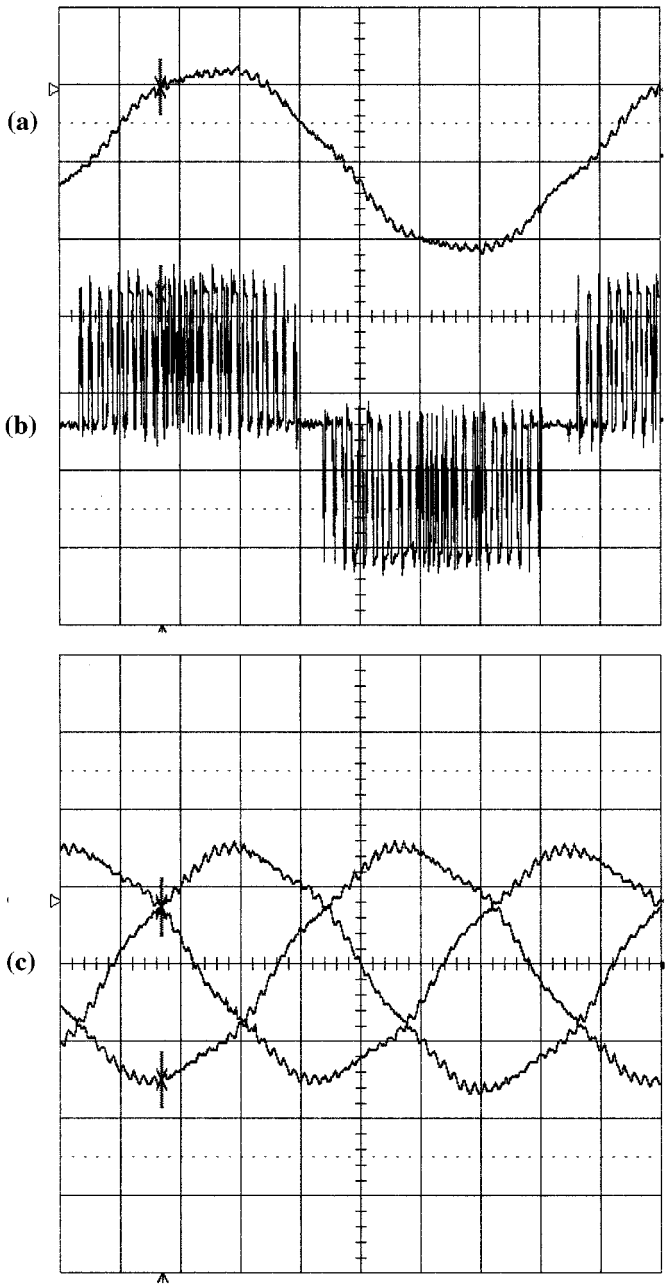

Fig. 15. Waveforms (2 ms/div) of (a) pulse width modulated phase current waveform (5 A/div), (b) load current waveform (2 A/div), and (c) three phase output line-line voltages (50 V/div) from the laboratory prototype actively commutated SCR-PWM inverter switching at 4 kHz.

VI. Conclusions

This paper has presented the realization of a pulse width modulated current source inerter. The converter is derived from the classical SCR based current source inverter by adding a gate-turn-off device on the dc bus, which enables active commutation of the inverter bridge. Experimental results verifying the operation of the active commutation of the inverter bridge have been presented, establishing the viability of the topology. The maximum switching frequency attainable using the proposed approach is directly related to the minimum time required by the SCRs to regain reverse blocking capability upon commutation. Typical inverter grade SCRs may permit switching frequencies of in the 3 to 5 kHz range without compromising the modulation process. A detailed analysis of the converter operation, establishing a basis for the modulation strategy was developed. The operation of the converter using the proposed modulator has been verified through computer simulations and experimental prototype. Successful commutation using the proposed modulation strategy requires output voltage of appropriate polarity to available to provide a reverse bias for the SCRs being turned off. This constrains the phase displacement between the output voltage and current waveforms to be within 30 degrees, lagging or leading. However, this limitation may be circumvented by modifying the realization of the dc side commutation switch.

The proposed PWM CSI offers significant advantages over more conventional CSI topologies. Some of the advantages include

a) rugged, high power, low cost thyristors can be used for bridge devices;
b) active commutation allows PWM operation;
c) uses SCRs inherent blocking capacity, no blocking diodes are needed unlike IGBT CSI.

The principle of active commutation presented in this paper can be used to realize PWM capability in a wide range of SCR based power conversion applications including rectifiers and cycloconverters and result in improved performance.

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