Modeling and Design of a Neutral-Point Voltage Regulator for a Three-Level Diode-Clamped Inverter Using Multiple-Carrier Modulation

Ashish Bendre, *Member, IEEE*, Giri Venkataramanan, *Member, IEEE*, Don Rosene, and Vijay Srinivasan, *Member, IEEE*

***Abstract*—The three-level diode-clamped multilevel converter commonly called the neutral-point-clamped converter has become established to be a preferred topology for high-power motor drive applications operating at several kilovolts. Although solutions to the problem of maintaining a stable neutral-point voltage in the converter continue to be the topic of research, a simple solution based on a design-oriented dynamic model of the system is not widely known. This paper presents the design, analysis, and implementation of a simple neutral-point voltage regulator for a three-level diode-clamped multilevel inverter, which uses a multiple-carrier sine-triangle modulator in conjunction with a closed-loop controller for neutral-point regulation. Redundant state choices are controlled via a continuous offset voltage that regulates the dc injection into the midpoint of the dc bus. A small-signal transfer function is developed in closed form, for neutral-point regulation, with the voltage offset as the control variable. Besides maintaining dc-bus voltage balance, the use of the approach leads to a significant reduction in the voltage distortion at the neutral point, allowing a definitive reduction in the required dc bus capacitance. Analytical, computer simulation, and experimental results verifying the approach are presented in this paper.**

***Index Terms*—Converter control, harmonics, modeling, modulation strategy, multilevel converters.**

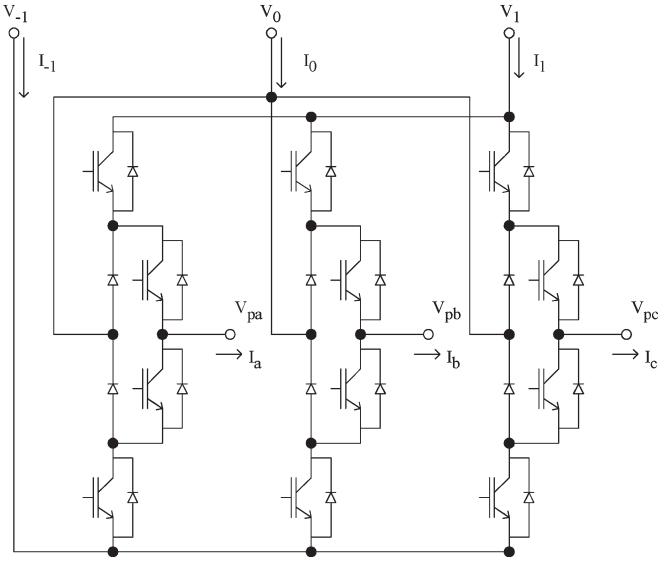

Fig. 1. Simplified schematic of the power circuit of a three-level neutral-point-clamped converter.

I. Introduction

THREE-LEVEL or neutral-point-clamped converters are seeing widespread application in large industrial drive systems [1], [2]. Several carrier-based and space-vector-based strategies have been proposed for the modulation of these converters [3], [4]. However, these strategies by themselves only concern themselves with output voltage waveform synthesis and require a *post facto* algorithm to manage the dc-bus power balance among the three-level dc. In general, they result in significant third-harmonic injection into the neutral point of the converter, which causes an increase in the required dc-link capacitance of the converter. Whereas a number of open-loop control strategies have been proposed for the reduction of the harmonic content [5], [6], a closed-loop control strategy, which reduces the harmonic content as well as regulates the neutral point from parasitic asymmetries like device voltage drops, is presented in this paper. The closed-loop regulator is based on controlling the neutral-point current injection as a function of a control input that corrects any existing imbalance. To assist the design of a stable regulator, small-signal transfer function models are necessary. Although extensive modeling has previously been carried out to predict the steady-state switching frequency effects of various modulators [7], [8], low-frequency dynamic models are not readily available for this purpose. This paper focuses on developing design-oriented models for use in the design of closed-loop compensators for multiple-carrier modulators, and loop stability is analyzed for low-frequency effects. A detailed simulation of a three-level inverter shows the operation of the closed-loop regulator for multiple-carrier modulation methods, and these results are verified using a hardware prototype. The partitioning of three-level inverter controller functions into output voltage synthesis and dc bus balance is described in Section II. Section III presents the relationships between the neutral-point current injection and the voltage offset provided to the three references. In Section IV,

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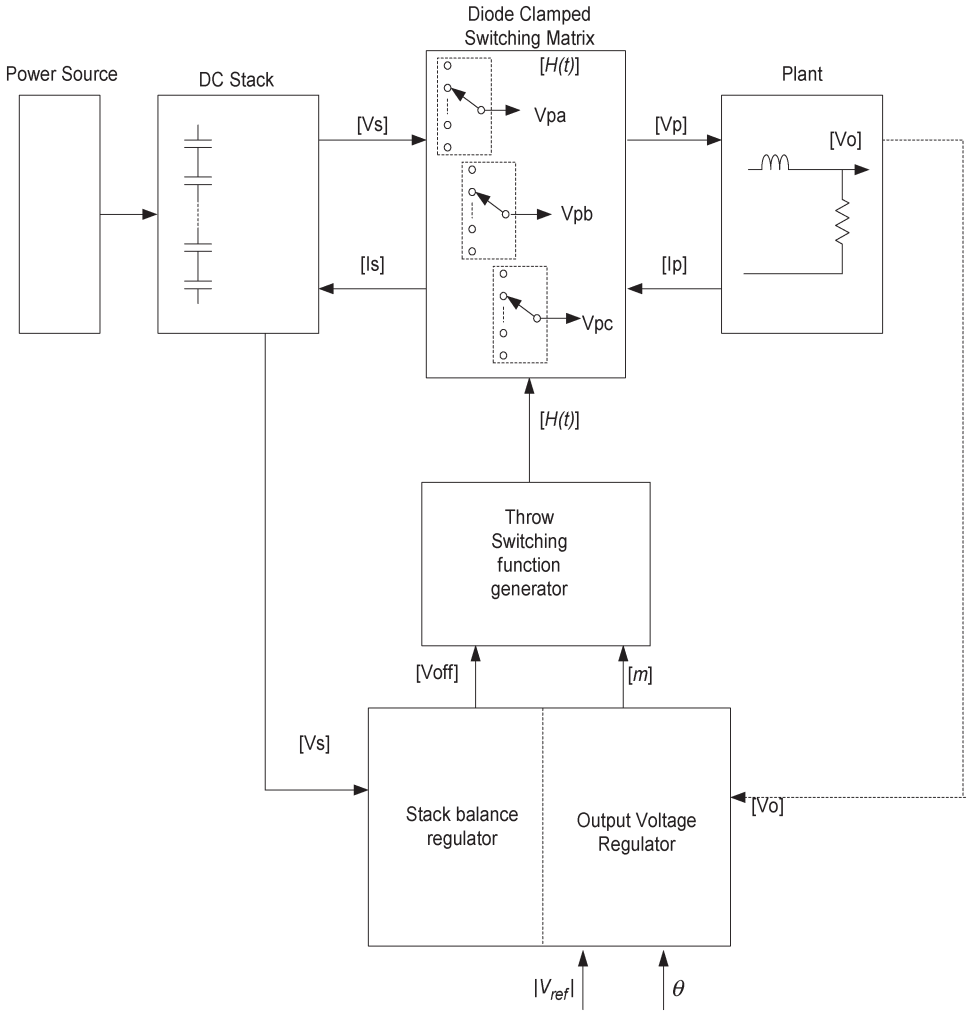


Fig. 2. Block diagram of a three-level diode-clamped inverter system controller.

the small-signal model for the controller is derived. Simulation results verifying the performance of the regulator and hardware results from a prototype three-level converter are included in Section V, followed by conclusions.

II. Closed-Loop Neutral-Point Regulator

A simplified schematic of the three-level neutral-point-clamped inverter is illustrated in Fig. 1. Fig. 2 shows a controller block diagram for a stacked multilevel inverter system where the major components of the system can be identified. The switching matrix $H(t)$ defines the input–output relationships between the various voltage levels of the dc stack to the three-phase currents. The load is modeled as resistive element in series with a filter inductor that yields sinusoidal output currents. The output voltages $V_o(t)$ and the stack voltages $V_s(t)$ are the feedback signals to the controller. The controller functions are partitioned into stack voltage balancing functions and output regulation. The output voltage regulator accepts output voltage reference magnitude $V_{\rm ref}$ and produces the three-phase pole voltage commands $m(t)$. Although the development here features an output voltage regulator, the neutral-point regulation algorithm may be implemented with motor drives with various open- or closed-loop regulation strategies. The dc stack balance regulator generates an offset voltage that is added to the reference waveforms of the pulsewidth modulator (PWM). Together, these are used to compute the individual elements of the switching matrix $H(t)$, which directly relate to the switch gating signals of the converter, as described in detail in [6].

The reciprocal properties of the switching matrix $H(t)$ of the multilevel converter connect the pole voltages and pole currents to the stack voltages and stack currents, which may be mathematically expressed as

$$\begin{aligned} V_p(t) &= H(t)V_s \\ I_s(t) &= H^T(t)I_p \end{aligned} \tag{1}$$

where

$$V_p(t) = [V_{\rm pa}(t) \quad V_{\rm pb}(t) \quad V_{\rm pc}(t)]^T \tag{2}$$

are the pole voltages

$$\begin{aligned} I_o(t) &= [I_a(t) \quad I_b(t) \quad I_c(t)]^T \\ &= I_{\rm pk}\left[\cos(t-\phi) \quad \cos\left(t-\phi-\frac{2\pi}{3}\right) \quad \cos\left(t-\phi+\frac{2\pi}{3}\right)\right]^T \end{aligned} \tag{3}$$

are the sinusoidal output currents

$$V_s(t) = [V_k(t) \quad V_{k-1}(t) \quad \cdots \quad V_{-k+1}(t) \quad V_{-k}(t)]^T \quad (4)$$

are the dc stack voltages

$$I_s(t) = [I_k(t) \quad I_{k-1}(t) \quad \cdots \quad I_{-k+1}(t) \quad I_{-k}(t)]^T \quad (5)$$

are the dc stack currents, and

$$H(t) = \begin{bmatrix} H_{Na} & H_{N-1a} & \cdots & H_{-N+1a} & H_{-Na} \\ H_{Nb} & H_{N-1b} & \cdots & H_{-N+1b} & H_{-Nb} \\ H_{Nc} & H_{N-1c} & \cdots & H_{-N+1c} & H_{-Nc} \end{bmatrix} \quad (6)$$

is the switching function matrix that connects the output ac poles to the various dc stack levels.

When the repetition frequency of the switching function is much larger than the power frequency of the desired ac output voltages, net power transfer between the dc voltages and the ac currents arises from the slowly varying average value of the switching functions. The average value of the switching functions may be readily represented by their time-varying duty ratio functions of the particular throw. The power transfer relationships of (1) may be approximated by

$$V_p(t) = M(t) \cdot V_s \quad (7)$$

and

$$I_s(t) = M(t)^T \cdot I_0(t) \quad (8)$$

where the elements m_{ij} of the modulation matrix $M(t)$ may be determined by computing the averaged duty ratio of the elements of the matrix $H(t)$. The averaging approximation used is an extension of multifrequency averaging used for dc–dc converters [9]

$$m_{ij}(\tau) = \frac{1}{T} \int_{\tau-T}^{\tau} H_{ij}(t)dt \quad (9)$$

with T being the switching period.

The generation of the modulating functions $m_{ij}(\cdot)$ from a set of reference voltage waveforms for the output voltage is performed using various modulation schemes. The use of multiple-carrier modulation schemes for synthesizing output voltage waveforms for these converters is well known [5], [6]. A representation of the carrier waveforms and the modulating signal for one of the three phases is illustrated in Fig. 3. It may be noticed that a voltage offset is added to the desired sinusoidal reference voltage, which plays the key role in regulating the neutral-point voltage. Thus, the reference voltages may be described by

$$\begin{aligned} V_a^{\text{ref}}(t) &= m\cos(t) + V_{\text{off}} \\ V_b^{\text{ref}}(t) &= m\cos\left(t - \frac{2\pi}{3}\right) + V_{\text{off}} \\ V_c^{\text{ref}}(t) &= m\cos\left(t + \frac{2\pi}{3}\right) + V_{\text{off}}. \end{aligned} \quad (10)$$

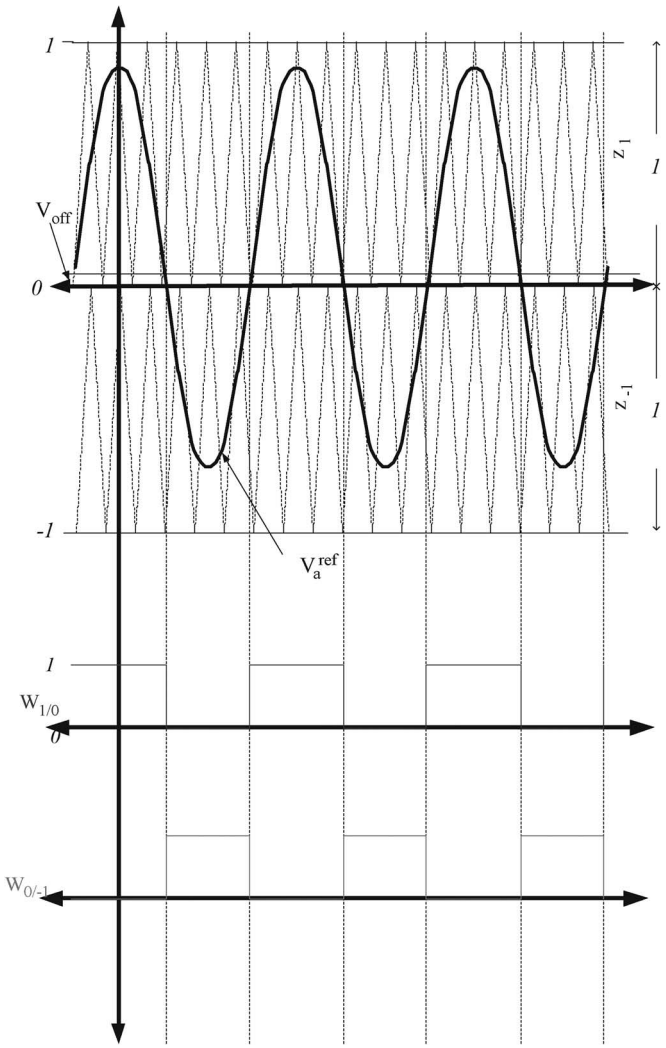


Fig. 3. Representative illustration of three-phase references, triangular carriers, and injected offset voltage of the multiple-carrier modulator for a three-level inverter.

Thus, the modulating functions are a function of modulation index m, time t, and the offset voltage V_{off}.

To obtain the dc stack current injection, (7) and (8) may be combined as

$$I_s(t) = [m_{ij}(t)]^T I_p(t) = [f_{ij}(m, V_{\text{off}}, t)]^T I_p(t). \quad (11)$$

Furthermore, if T_f is the period of the fundamental output voltage waveform, the average stack injection may be expressed as

$$\begin{aligned} \text{Avg}\,[I_s(t)] &= \frac{1}{T_f} \int [m_{ij}(t)]^T I_p(t)dt \\ &= \frac{1}{T_f} \int [f_{ij}(m, V_{\text{off}}, t)]^T I_p(t)dt. \end{aligned} \quad (12)$$

By normalizing the period T_f to 2π, which is the equivalent of normalizing the angular frequency ω to unity, the angle variable becomes θ.

The dc current injection obtained from the reciprocity equation can be integrated over fundamental period to compute the

average current sourced from a given stack, i.e.,

$$I_i^{\mathrm{AVG}} = \frac{1}{2\pi}\int_0^{2\pi} \left(m_{ia}(\theta)I_a(\theta) + m_{ib}(\theta)I_b(\theta) + m_{ic}(\theta)I_c(\theta)\right) d\theta. \tag{13}$$

As the lowest harmonic component is the third harmonic and all harmonics are triple, integrating over $2\pi/3$ is sufficient, i.e.,

$$I_i^{\mathrm{AVG}} = \frac{1}{2\pi/3}\int_0^{2\pi/3} \left(m_{ia}(\theta)I_a(\theta) + m_{ib}(\theta)I_b(\theta) + m_{ic}(\theta)I_c(\theta)\right) d\theta. \tag{14}$$

The design of the regulator follows two sequential steps. First, the input–output relationship between the V_{off} and the dc stack current injection as a function of operating conditions such as modulation level, output current, and power factor is determined by applying the generalized multilevel switching function model to three-level converters. This nonlinear function is then linearized at the steady-state operating condition and used for developing a controller for the stack voltages. These developments are described in the following sections.

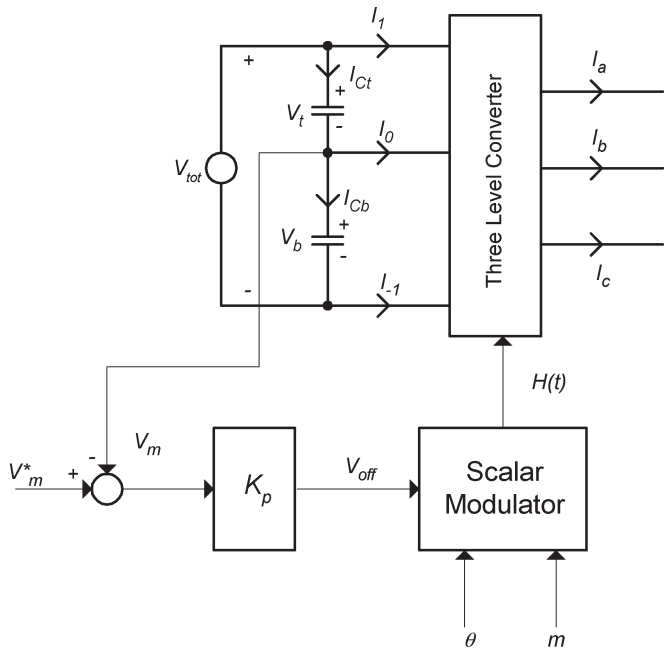


Fig. 4. Schematic representation of the proposed neutral-point voltage regulator including the dc-link section of the power circuit of the three-level inverter.

III. Modeling DC Stack Current Injection for Three-Level Converters

Multiple-carrier modulation technique for a three-level converter consists of two triangular waveforms with identical peak–peak values as illustrated in Fig. 3. The peak–peak value of each carrier waveform is one. The waveforms divide the vertical space into two zones (z_1, z_{-1}), each one corresponding to a distinct throw of the single-pole multiple-throw switch. The throws of the switch are operated such that when the modulating function of the particular phase is in a particular zone, the throw corresponding to that zone is turned on.

The modulation technique described previously may be modeled mathematically to the extent that the modulation functions for each throw of the switch can be determined from the value of the desired output voltage reference waveform. For this purpose, the interval [1, −1] is divided into two windows. The windows are labeled $(W_{1/0}, W_{0/-1})$. A membership function for the modulating signal corresponding to each window can be defined as being unity when the signal occupies that window and zero otherwise.

For scalar modulation, the throw functions for a given phase depend entirely on the phase reference itself. The window functions that comprise the expression for the throw functions are dependent on just one phase reference also. The window functions, which are a function of one variable, can be described by the following relationship. Each window is an interval in the range of the reference function $V_a^{\mathrm{ref}}(t)$ as shown in the following:

$$\begin{aligned} W_{1/0}^a(t) &= 1, \qquad \text{if } 0 < V_a^{\mathrm{ref}}(t) < 1 \\ W_{1/0}^a(t) &= 0, \qquad \text{otherwise.} \end{aligned} \tag{15}$$

Similarly

$$\begin{aligned} W_{0/-1}^a(t) &= 1, \qquad \text{if } 0 < V_a^{\mathrm{ref}}(t) < 1 \\ W_{0/-1}^a(t) &= 0, \qquad \text{otherwise.} \end{aligned} \tag{16}$$

When the modulator is not saturated, the modulating signals $V_a^{\mathrm{ref}}(t)$, $V_b^{\mathrm{ref}}(t)$, and $V_c^{\mathrm{ref}}(t)$ always fall within the interval [1, −1]. For each phase, the membership function corresponding to one window will be unity and every other one zero. An example of the windows, modulating signal, and its membership function for a three-converter phase is illustrated in the lower two traces of Fig. 3.

Using this definition of the window membership function, the averaged duty ratio matrix for a three-phase three-level converter can be expressed as (17), shown at the bottom of the page.

$$M^3(t) = \begin{pmatrix} V_a^{\mathrm{ref}}(t)W_{1/0}^a & \left(1 - V_a^{\mathrm{ref}}(t)\right)W_{1/0}^a + \left(1 + V_a^{\mathrm{ref}}(t)\right)W_{0/-1}^a & -V_a^{\mathrm{ref}}(t)W_{0/-1}^a \\ V_b^{\mathrm{ref}}(t)W_{1/0}^b & \left(1 - V_b^{\mathrm{ref}}(t)\right)W_{1/0}^b + \left(1 + V_b^{\mathrm{ref}}(t)\right)W_{0/-1}^b & -V_b^{\mathrm{ref}}(t)W_{0/-1}^b \\ V_c^{\mathrm{ref}}(t)W_{1/0}^c & \left(1 - V_c^{\mathrm{ref}}(t)\right)W_{1/0}^c + \left(1 + V_c^{\mathrm{ref}}(t)\right)W_{0/-1}^c & -V_c^{\mathrm{ref}}(t)W_{0/-1}^c \end{pmatrix} \tag{17}$$

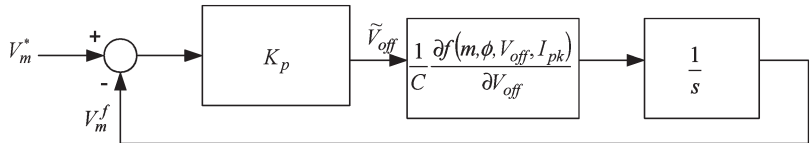


Fig. 5. Simplified representation of the closed-loop neutral-point regulator.

Substituting into (14), the average neutral-point current can be expressed in (18)

$$\begin{aligned} I_0^{\mathrm{AVG}} &= \frac{1}{2\pi/3} \\ &\times \int_0^{2\pi/3} \Big(\Big(\big(1 - V_a^{\mathrm{ref}}(t)\big) W_{1/0}^a + \big(1 + V_a^{\mathrm{ref}}(t)\big) W_{0/-1}^a \Big) I_a(t) \\ &\quad + \Big(\big(1 - V_b^{\mathrm{ref}}(t)\big) W_{1/0}^b + \big(1 + V_b^{\mathrm{ref}}(t)\big) W_{0/-1}^b \Big) I_b(t) \\ &\quad + \Big(\big(1 - V_c^{\mathrm{ref}}(t)\big) W_{1/0}^c + \big(1 + V_c^{\mathrm{ref}}(t)\big) W_{0/-1}^c \Big) I_c(t) \Big) dt. \end{aligned} \tag{18}$$

The integral (18) contains three symmetric terms. If a process for evaluating one term is demonstrated, it can then be expanded to include the contributions of the other two terms in the expression. The first term, which is the contribution due to the a phase, can be expressed as

$$I_{0a}^{\mathrm{AVG}} = \frac{1}{2\pi/3} \int_0^{2\pi/3} \Big(\big(1 - V_a^{\mathrm{ref}}(t)\big) W_{1/0}^a + \big(1 + V_a^{\mathrm{ref}}(t)\big) W_{0/-1}^a \Big) I_a(t) dt. \tag{19}$$

As the window functions are binary in nature, they can be reduced to limits for the integral evaluation as

$$I_{0a}^{\mathrm{AVG}} = \frac{1}{2\pi/3} \left(\int_0^{(\pi/2)-\beta} \big(1 - V_a^{\mathrm{ref}}(t)\big) I_a(t)\, dt + \int_{(\pi/2)-\beta}^{2\pi/3} \big(1 + V_a^{\mathrm{ref}}(t)\big) I_a(t)\, dt \right)$$

$$\text{where } \beta = \frac{\pi}{2} - \cos^{-1}\left[\frac{V_{\mathrm{off}}}{m}\right]. \tag{20}$$

It can be observed that when the offset voltage is zero, β equals $\pi/2$, which is expected for a cosine reference. If the phase currents are expressed as in (4) and the contributions from the other two phases included, the average neutral-point current can be shown to be

$$I_0^{\mathrm{AVG}} = \frac{3}{\pi} \cos(\phi) I_{pk} \left[m\beta - (2V_{\mathrm{off}} + m \sin\beta) \cos\beta \right] \tag{21}$$

with β defined in (20). Note that the neutral-point current is identically equal to zero when the offset voltage is set to zero. This corresponds to the normal open-loop operation.

This development shows that using a neutral-point regulator that adds an offset term to all three references influences the window membership functions and hence the limits on the integrals in (18). If the references are balanced sinusoids, these limits will correspond to fixed angles; however, when the offset is added to the references, these limits will be a function of both the reference sinusoid as well as the offset term. Having developed the neutral-point current injection as a function of the operating conditions and the control input V_{off}, the regulator design may be developed as described in the following section.

IV. Regulator Design

A schematic representation of the neutral-point regulator including the section of the dc-link elements of the multilevel inverter is highlighted in Fig. 4. From the equivalent circuit, the dynamics of the voltage imbalance V_m $(= V_t - V_b)$ may be expressed as

$$\frac{dV_m^{\mathrm{AVG}}}{dt} = \frac{1}{C} \left(I_0^{\mathrm{AVG}} \right) \tag{22}$$

where

$$I_0^{\mathrm{AVG}} = f(m, \phi, V_{\mathrm{off}}, I_{pk}) \tag{23}$$

as described in (21). The small-signal behavior of this system with respect to the control input being the sharing function may be characterized as follows:

$$C \frac{d\widetilde{V}_m^{\mathrm{AVG}}}{dt} = \frac{\partial f(m, \phi, V_{\mathrm{off}}, I_{pk})}{\partial V_{\mathrm{off}}} \widetilde{V}_{\mathrm{off}} \tag{24}$$

where

$$\frac{\partial I_0^{\mathrm{AVG}}}{\partial V_{\mathrm{off}}} = -6 I_{pk} \cos(\phi) \left[\frac{m^2 - 3V_{\mathrm{off}}^2}{m^2 \pi \sqrt{1 - \frac{V_{\mathrm{off}}^2}{m^2}}} \right]. \tag{25}$$

From (22) and (25), it is clear that the small-signal dynamics of the neutral-point voltage are represented by an integrator whose gain depends on the partial derivatives expressed by (25) with respect to the offset voltage. Thus, the system will have zero steady-state error dynamics using only a proportional controller with gain K_p as shown in Fig. 5. It is seen that the forward gain is dependent on the magnitude and phase of the reference vector, and the sign is dependent on the power factor. Thus, *a priori* knowledge of the power delivery mode (motoring or regenerating) is required to design a stable compensator. The

TABLE I
PARAMETERS FOR PROTOTYPE THREE-LEVEL INVERTER SYSTEM

Parameter	Value
Load Inductance	12mH
Load Resistance	25 Ω
DC Link Voltage	400 V
Output current	5 A
DC bus capacitance	90 μF
Switching frequency	5 kHz
Modulation level	0.75
Bandwidth of neutral point regulator	200 Hz

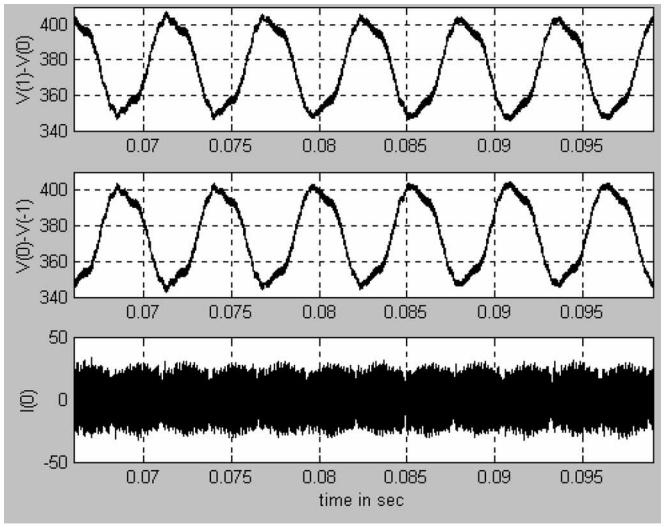
closed-loop transfer function between the command voltage and actual imbalance may be expressed as

$$\frac{V_m^f}{V_m^*}(s) = \frac{1}{1+\frac{s}{K_p\left(\partial I_0^{\mathrm{AVG}}/\partial V_{\mathrm{off}}\right)}} = \frac{1}{1+\frac{s}{K_p(\partial f(m,V_{\mathrm{off}},I_{pk},\phi)/\partial V_{\mathrm{off}})}}. \quad (26)$$

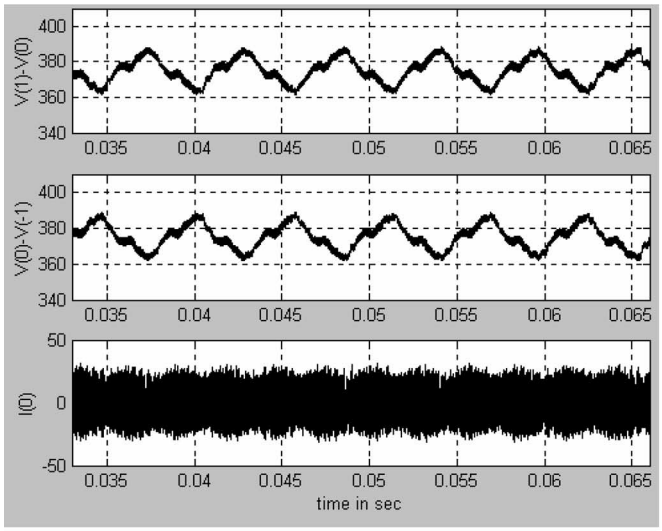
The closed-loop system transfer function is that of a low-pass filter with a bandwidth controlled by the gain K_p. Clearly, the bandwidth of the neutral-point regulator can be improved by increasing the proportional gain of the compensator. If the value of gain K_p is increased to be large enough such that the bandwidth is greater than the third-harmonic frequency (typically 180 Hz), the neutral-point regulator will be capable of decreasing the third-harmonic voltage ripple. This serves as the guideline for selecting the value of K_p. If the current phase angle and amplitude are known, the compensator gain can be dynamically scheduled to compensate for the variations in the system forward gain, thus ensuring a uniform bandwidth of about 200 Hz under various operating conditions. This nominal bandwidth was chosen in the illustrative example system described in the following section.

V. SIMULATION AND HARDWARE RESULTS

A MATLAB Simulink [10] model of a three-level converter using multiple-carrier modulation was developed and operated in inverter mode. The operating parameters are shown in Table I. Extensive simulations were conducted to verify the performance of the regulator and the inverter system at a wide variety of operating conditions. Selected waveforms from the computer simulation are illustrated in Fig. 6, which shows the upper and lower bus voltages and the zero neutral-point current injection, with and without a neutral-point regulator. The control waveform V_{off} can be interpreted from this plot as a signal proportional to the difference between the upper and lower dc buses. The superior performance of the system using the closed-loop neutral-point regulator is readily evident from the figure.



(a)

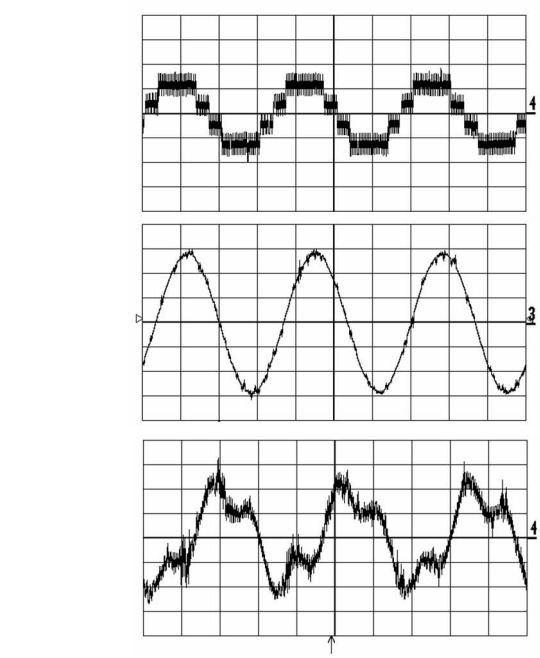


(b)

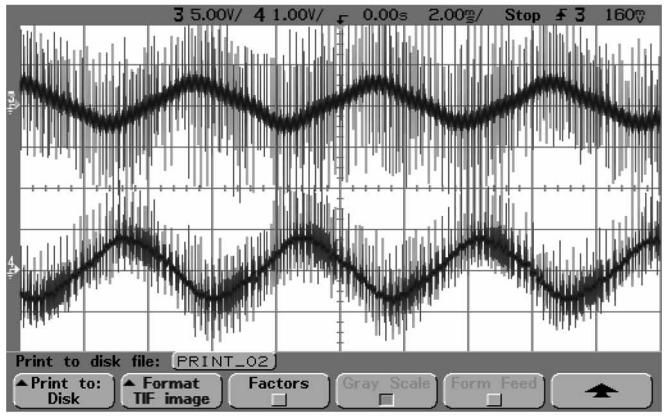
Fig. 6. Waveforms (5 ms/div) obtained from the simulation of the three-level inverter (a) without neutral-point regulation and (b) with neutral-point regulator. Top traces: Upper-level dc-bus voltage (5 V/div). Bottom traces: Neutral-point current (1 A/div).

A hardware prototype was built to verify the analysis and simulation results obtained using the closed-loop neutral-point regulator. The prototype used nine dual insulated gate bipolar transistor (IGBT) devices and unlytic capacitors interconnected with laminated bus planes to create a three-phase three-level inverter power platform. The control algorithm has been implemented on a general-purpose real-time control prototyping platform. This platform is based on a TI TMS320C31 Digital Signal Processor and a Xilinx Spartan series Field Programmable Gate Array for software and logic-based algorithm implementation. Key operating waveforms from the hardware prototype, i.e., pole a–pole c voltage, load line–line voltage, etc., are shown in Fig. 7.

The analytically derived small-signal model of the offset-based neutral-point regulator was verified by using a closed-loop frequency response analyzer [11]. This instrument is used to inject a small disturbance into the error signal of the



(a)



(b)

Fig. 7. Hardware prototype experimental waveforms of (a) output pole–pole voltage (top trace, 5 ms/div, 250 V/div), sinusoidal load line–line voltage (middle trace, 5 ms/div, 100 V/div), and neutral-point current (bottom trace, 5 ms/div 1 V/div) normalized modulating waveform for A phase, illustrating the third-harmonic offset voltage superimposed on the fundamental component; and (b) neutral-point voltage (top trace, 2 ms/div, 5 V/div) and controller offset voltage V_{off} (2 ms/div, 1 V/div), illustrating third-harmonic components.

neutral-point regulator while the closed loop is operational. By measuring the response of the neutral-point regulator to the injected disturbance, the loop gain of the system can be measured directly. The predicted results from the mathematically derived small-signal model of Fig. 5 show excellent match with the actual measurements as seen in Fig. 8.

The loop gain figures show that for the given system parameters, the regulator exhibits a finite nonzero gain even out to the third-harmonic frequency. Thus, the regulator action reduces the neutral-point current ripple at the third harmonic as seen from the current measurements shown in Fig. 9(a). The spectral plot of neutral-point current shown in Fig. 10 confirms the activity of the neutral-point regulator at the third harmonic as significant attenuation is seen. This action also reduces the

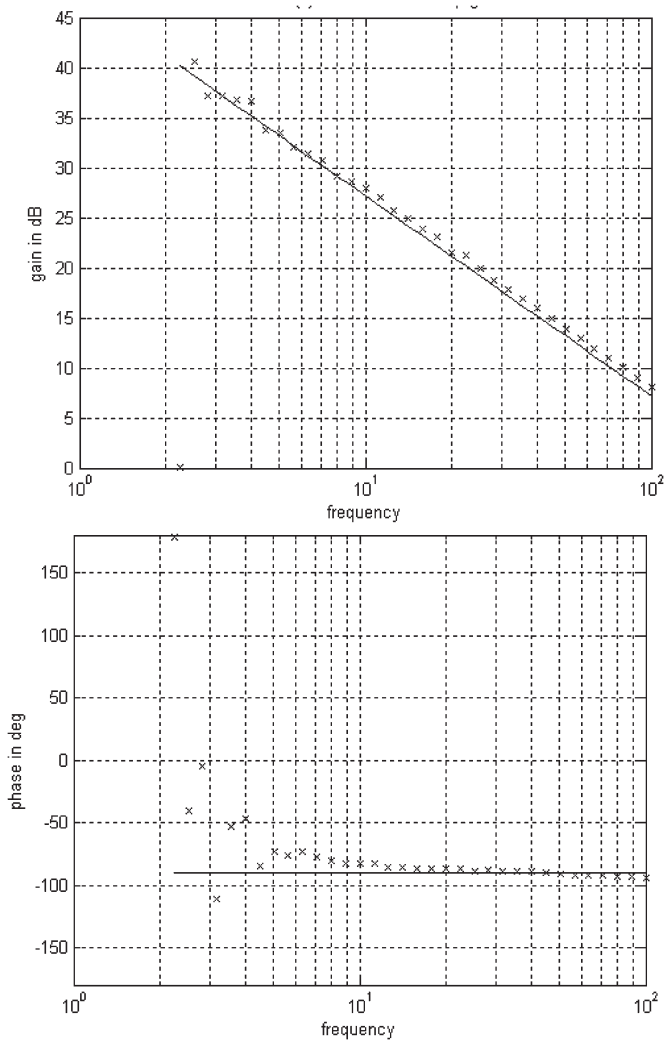


Fig. 8. Analytical calculations (solid line) and experimental measurements ($\times$ points) of small-signal loop gain of the neutral-point regulator.

ensuing neutral-point voltage ripple as seen in Fig. 11, which shows the measured upper dc bus waveform (ac coupled) along with the offset command with and without the closed-loop neutral-point voltage regulator.

VI. Conclusion

This paper has presented a neutral-point voltage regulator for a three-level diode-clamped multilevel converter, which uses a multiple-carrier modulator in conjunction with a voltage-offset-based neutral-point balance controller. This combined control approach does not compromise the output voltage synthesis function while maintaining tight regulation of the neutral-point voltage even with a small dc-link capacitance. A voltage offset added to all three-phase references is used as a control handle to vary the ratio of distribution of duty cycles of redundant. Closed-form expressions are presented for the neutral-point current injection as a function of the modulation index, the power factor, and the offset voltage. By analyzing small-signal models for the neutral-point voltage developed using these closed-form expressions, a closed-loop neutral-point compensator has been designed that provides excellent performance

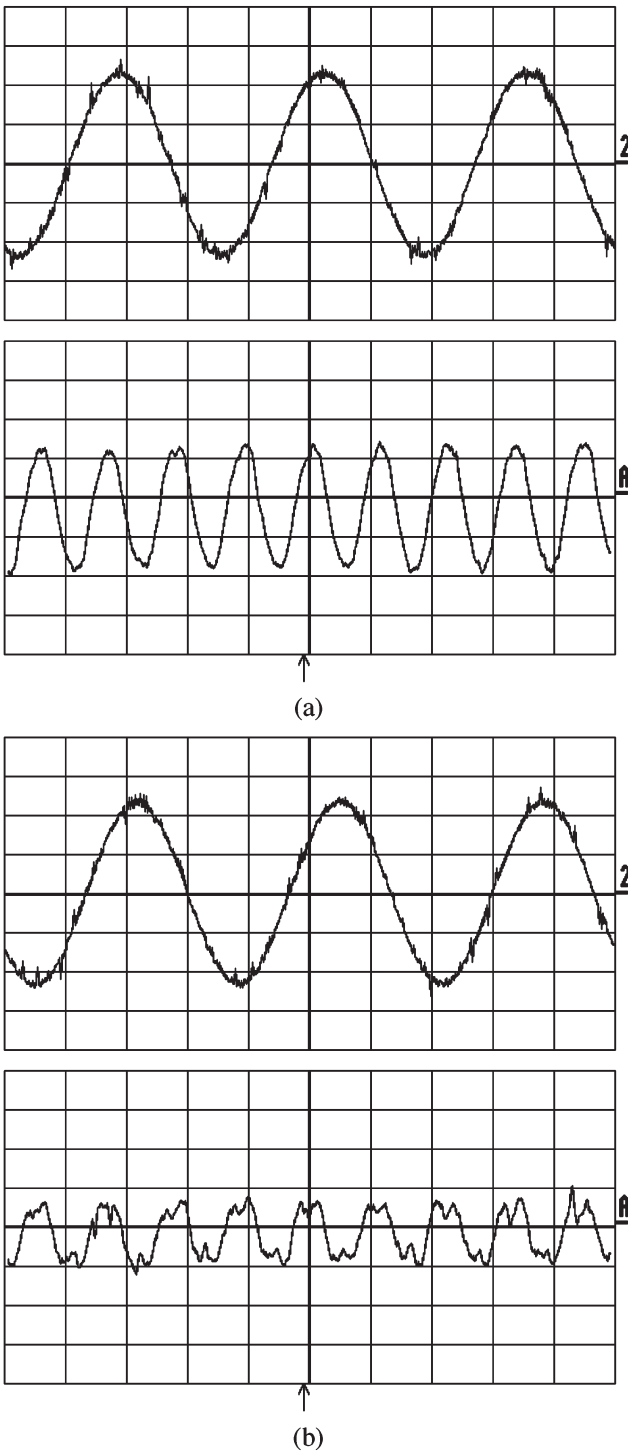


Fig. 9. Hardware prototype experimental waveforms (at 5 ms/div) from the system (a) without neutral-point regulator [phase current (top traces, 2 A/div) and filtered neutral-point currents (bottom traces, 2 A/div)] and (b) with neutral-point regulator [phase current (top traces, 2 A/div) and filtered neutral-point currents (bottom traces, 1 A/div)].

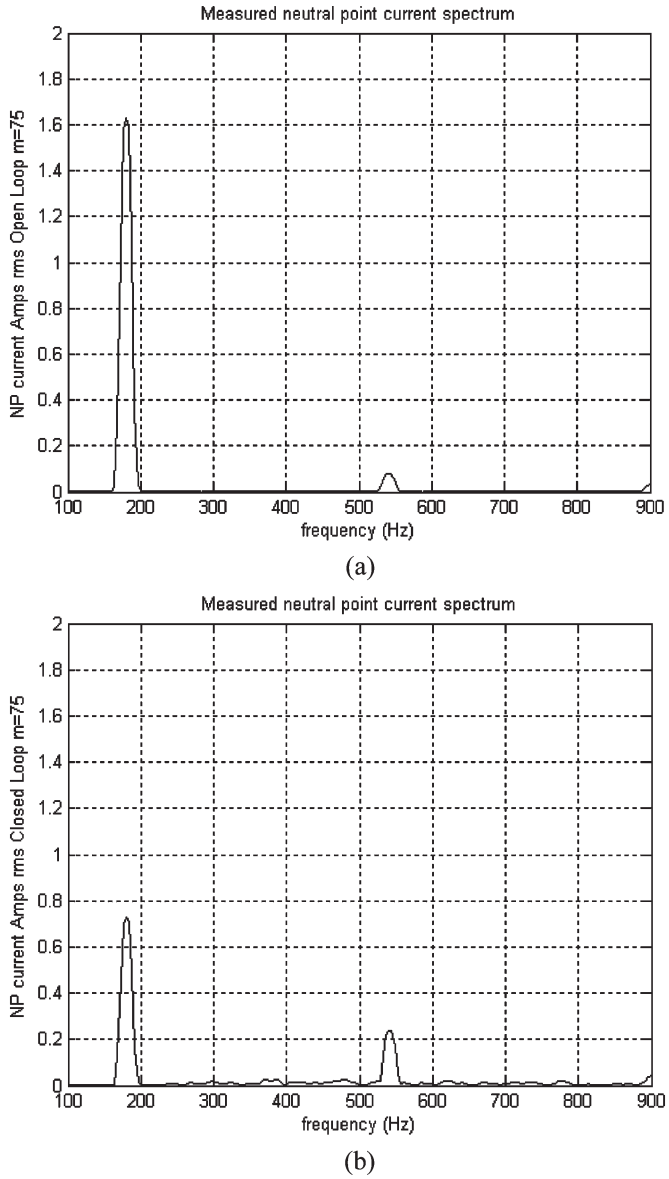
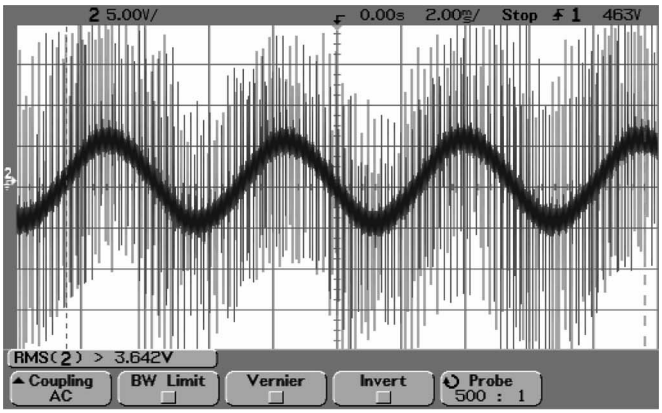
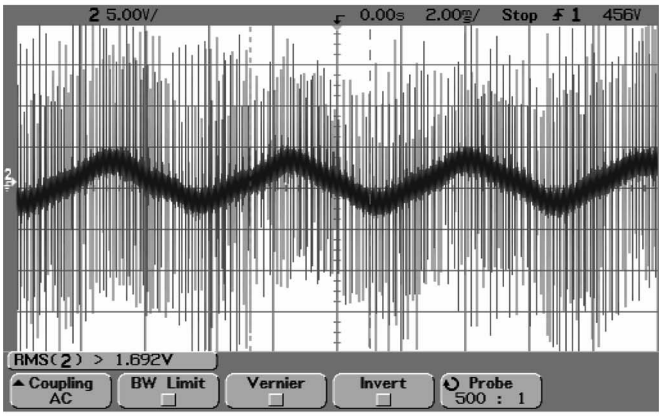


Fig. 10. Measured waveforms from hardware prototype operating as in Fig. 9: frequency spectrum of neutral-point current (a) with regulation and (b) without regulation.

and stability. A detailed computer simulation of a three-level inverter with very modest dc bus capacitance is implemented in MATLAB Simulink, and the neutral-point voltage waveforms have been presented. Measured waveforms from a three-level hardware prototype show very close correlation to analytic and simulation results. Very close match is seen between predicted and measured loop gains for the neutral-point compensator. A significant improvement is seen in the voltage distortion at the neutral point when the regulator is used, and this leads to a definitive reduction in the required dc-bus capacitance. The prototype converter utilized a value of 90 μF of film capacitance, whereas use of 1000 s of μF is most common in the state of the art. The proposed strategy has been extended to space-vector PWM strategies producing effective neutral-point regulators, and these results will be presented in a future publication. The novel concept of controlling the neutral-point injection via a continuous voltage offset, and then developing small-signal models for closed-loop regulators with this sharing function as the control variable, can also be applied to regulate other system quantities such as the speed of the drive motor, dc bus voltage in the case of rectifier mode of operation, etc. Detailed analytical development and experimental results verifying the performance have been presented in this paper.



(a)



(b)

Fig. 11. Measured waveforms from hardware prototype operating as in Fig. 9: ac-coupled upper dc-bus voltage (2 ms/div, 5 V/div) illustrating reduction of third-harmonic ripple voltage (a) without neutral-point regulation and (b) with neutral-point regulation.

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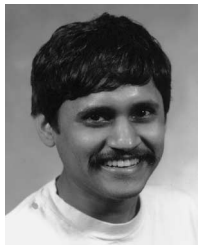

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