Plasma-Parameter Dependence of Thin-Oxide Damage from Wafer Charging During Electron-Cyclotron-Resonance Plasma Processing

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***Abstract*—In this work, the effects of plasma-parameter variations on charging damage to polysilicon-gate MOS capacitor test structures exposed to O_2 electron-cyclotron-resonance (ECR) plasmas are investigated. Results will show that charging damage is generated when large potential differences exist across the gate-oxide layers of the MOS capacitor test structures and that these potential differences can only occur in the presence of plasma nonuniformities. These results demonstrate the critical need for plasma uniformity during processing, in particular as device dimensions shrink and gate-oxide thicknesses decrease. The plasma parameters were varied by adjusting the neutral gas pressure and by independently biasing a circular grid and a ring electrode located above the wafer. The damage induced in the test wafers during the plasma exposure was characterized with ramp-voltage breakdown measurements. Radial profiles of the floating potential measured with a Langmuir probe were found to vary nonuniformly when the grid electrode was positively biased due to preferential depletion of electrons relative to ions beneath the grid electrode. An equivalent-circuit model of the test wafer and the wafer-stage electrode predicts that the silicon substrate acquires a potential equal to the average of the wafer surface potential. Comparisons of the calculated profiles of the potential difference across the gate-oxide layers of the test structures and whole-wafer maps of the breakdown-voltage measurements show that the majority of the damage occurs where the oxide potential difference is largest and that the damage only occurs in the presence of plasma nonuniformities.**

I. Introduction

ELECTRON-cyclotron-resonance (ECR) plasma reactors operate at high plasma densities ($>10^{11}$ cm^{-3}) and low neutral pressures ($\approx 10^{-3}$ Torr) and are being used for ultra large scale integration (ULSI) manufacturing as remote plasma sources for etching and thin-film deposition applications, [1]–[6]. Their high degree of ionization ($>10\%$) and concomitant high free-radical densities, combined with a plasma generation mechanism that is independent of substrate biasing, are of intrinsic advantage for submicron processing with high etch rates.

As critical device dimensions shrink to one-quarter μm and below and gate-oxide thicknesses decrease below 10 nm, ULSI yields will be increasingly limited by plasma-induced damage. This damage is the result of exposure to the various particle and energy fluxes present in the plasma environment and for gate oxides can be caused by wafer surface charging, [7]–[9]. The damage generated by this charging is the result of Fowler–Nordheim (F–N) current stressing of thin oxides under floating gates, [10], [11].

The goal of this research is to investigate charging damage to polysilicon-gate metal-oxide-semiconductor capacitor test structures upon exposure to O_2 plasmas generated in an ECR plasma source. In particular, we are interested in determining the relationship between the plasma conditions and the degree of process-induced damage, as previous work in ECR reactors [12]–[14], and other types of plasma systems [15]–[18], has indicated that nonuniformities in the plasma parameters across the surface of the wafer during processing can play a major role in the generation of charging damage. In order to minimize (or significantly reduce) the number of experimental measurements and test wafers needed to establish this relationship, we have developed a method for expediently adjusting both the nonuniformities and spatial averages of the plasma parameters across the surface of the wafer.

In this method, a circular grid and a ring electrode (or dual-electrode assembly) are immersed in the plasma during processing. The electrodes are electrically isolated both from each other and the vacuum chamber, and can be independently biased. By adjusting the operating parameters of the ECR reactor and the magnitudes of the electrode biases, it is possible to alter the nonuniformities and spatial averages of the plasma parameters. Wafers containing MOS capacitor test structures were exposed to different plasma conditions generated by adjusting the operating parameters of the ECR system and the dual-electrode assembly. The plasma conditions were characterized with Langmuir probe measurements and the process-induced damage was determined from breakdown voltage measurements of the individual MOS capacitor test structures.

To relate the measurement of the plasma parameters and the breakdown voltages to each other, an equivalent-circuit model of the test wafer and the wafer-stage has been developed.

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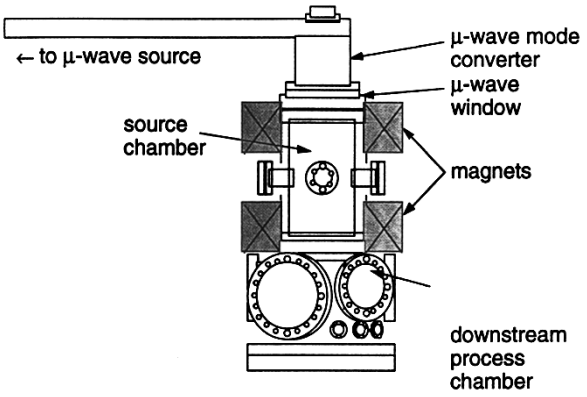

Fig. 1. The electron-cyclotron-resonance plasma etching system.

This model shows that the potential of the silicon substrate is approximately equal to the average potential across the surface of the wafer and allows the potential difference across the gate-oxide layers of the test structures to be calculated. When the calculated profiles of the oxide potential difference are compared with whole-wafer maps of the breakdown-voltage measurements, the maximum damage is seen to occur where the oxide potential difference is largest, but only in the presence of plasma nonuniformities.

II. Experimental Setup

A. Description of the ECR Plasma Source and Langmuir Probe Diagnostic

The ECR plasma etching system employed in this research consists of a source region where the electron cyclotron resonance is maintained and a downstream target region where the wafer may be positioned for etching (see Fig. 1). The ECR source is commercially manufactured (ASTeX model S-1500i) and consists of a 1.5 kW 2.45 GHz microwave power supply, vacuum chamber, waveguide, rectangular-to-circular microwave mode converter (TE_{10} to TM_{01}), magnet power supplies, and a pair of magnets arranged in a magnetic-mirror configuration. An anodized aluminum liner is positioned inside the source region, reducing sputtering of the stainless steel reactor walls and providing an electrically floating boundary to the plasma. The downstream vacuum chamber includes a load-lock and a magnetically coupled linear feed-through to reduce contamination while transferring wafers into and out of the system. Once in the system, wafers rest on a stage which has provisions for applying rf power, electrostatic clamping, and helium backside cooling to the wafer. In addition, the position of the sample stage can be varied along the axis of the system.

Gas is introduced into the system with mass flow controllers through a gas-distribution ring near the microwave window. The chamber pressure is monitored in the source and downstream regions with capacitance manometers. The system is pumped by a Leybold turbomolecular pump with a pumping speed of 1000 l/s. The operating pressure ranges from 0.5–10 mTorr with gas flow rates of up to 100 sccm per gas. A throttle valve located at the throat of the turbomolecular pump provides for independent control of the operating pressure and the gas flow rates.

Probe data was taken with a data-acquisition system consisting of a personal computer, a 12-b data-acquisition board, a probe-driver circuit, and the Langmuir probe. The probe-driver circuitry provides a voltage in the range of ± 125 V and is controlled by the computer via a 12-b digital-to-analog converter, yielding a voltage resolution of 61 mV. The probe current is determined by passing the current through a resistor, which is chosen to produce a ± 10-V signal at full-scale current. This voltage is delivered to a 12-b analog-to-digital converter through an isolation stage. When the resistor is 100 Ω, the full-scale current range is ± 100 mA and the current resolution is 49 μA. The probe driver is designed so that the voltage at the probe tip is not affected by the voltage drop across the current-sensing resistor. The tips of the Langmuir probe were planar with a diameter of $1/8$ in. and made from stainless steel (which proved to be the best material for use in an oxygen plasma environment, as probe tips made of tungsten and tantalum quickly developed an oxidized surface layer). Probe traces were analyzed using a nonlinear fitting algorithm which has been described previously [19]. In this algorithm, a two-temperature Maxwellian model is used to fit the data and determine the plasma potential, electron temperatures and current ratio of the two Maxwellian electron distributions. The floating potential is determined directly from the data as the voltage where the probe current is zero. The ion current is found by fitting the data in the ion-saturation region of the probe trace using a square-root dependence for the probe voltage, while the electron current is found after the fitted ion current is subtracted from the probe trace. The plasma density is determined using the fitted ion-saturation current and electron temperatures.

B. Wafer Test Structure and Measurements

The damage test structures used in this work were polysilicon-gate MOS capacitors. A diagram of the test structure is shown in Fig. 2. This type of capacitor test structure, commonly called an "antenna," (but more aptly described as a "charge collector") consists of a conductor (gate) which extends over both a thin gate oxide and a thick field oxide. Its purpose is to simulate the charge collection of a floating interconnect connected to the gate of a MOS transistor. Consequently, the thin-oxide area (A_g) is usually kept small, near that of a minimum-sized transistor gate, while the area of the polysilicon antenna (A_f), which is the portion of the polysilicon on top of the thick field oxide, is made much larger than the thin-oxide area. Often antenna structures are characterized by the ratio A_f/A_g, with values between 10^4–10^5 typically quoted as the minimum ratio before evident charging damage is allowed for a given process.

The MOS capacitor antenna structures were fabricated on n-type Si wafers with a diameter of ten centimeters, a resistivity of 5 Ω-cm, and a crystal orientation of $\langle 100 \rangle$. The fabrication process consisted of: 1) wet oxidation of the thick field oxide at 1000 °C;, 2) photoresist deposition and lithography patterning of the active area of the capacitor gate; 3) buffered HF etch

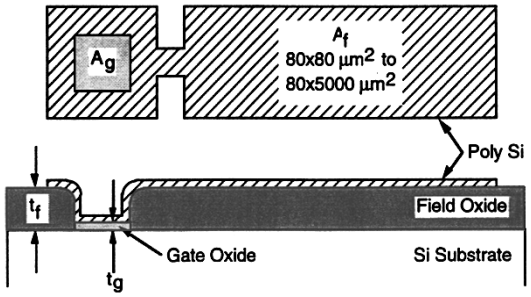

Fig. 2. Cross section and top view of the MOS capacitor test structure showing the Si substrate, field and gate oxides, and the polysilicon gate. Also indicated are: t_f, the thickness of the field oxide, t_g, gate-oxide thickness, A_f, the area of the polysilicon that is over field-oxide, and A_g, the area of the polysilicon covering the gate oxide.

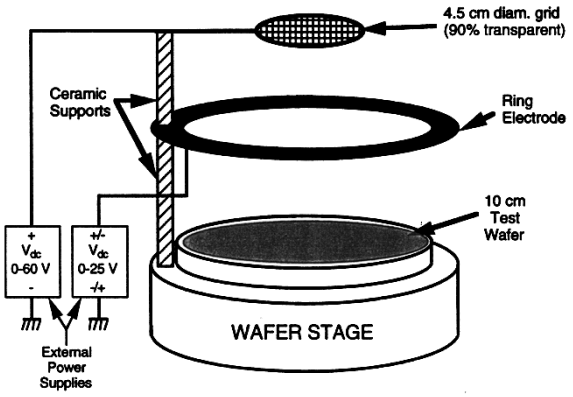

Fig. 3. Diagram of dual electrode assembly used to control the radial plasma uniformity. The ring and grid electrode are biased independently with external power supplies.

of the future thin-oxide area to avoid any plasma damage to the Si substrate; 4) thin-oxide growth at 850 °C; 5) blanket deposition of the polysilicon followed by a n-type doping and two hour annealing step at 900 °C; 6) photoresist deposition and lithography patterning of the polysilicon gate; and 7) wet etching to define the polysilicon gate.

The polysilicon charge-collecting area (A_f) varied from 0.064–0.4 mm^2 with two different gate oxide areas (A_g) of $6 \times 6\,\mu$m^2 and $20 \times 20\,\mu$m^2. Given these values, the antenna ratio varies from 16–1,000 for the $20 \times 20\,\mu$m^2 gate and from 178–11 111 for the $6 \times 6\,\mu$m^2 gate. In addition the gate-oxide thickness (t_g) is 10 nm and the field-oxide thickness (t_f) is 500 nm. Note that the gate oxide is fully covered, and thus protected from direct ultraviolet radiation and electron bombardment from the plasma. On a single die, there are 11 different antenna sizes for each different gate-oxide area (20×20 and 6×6). Each of these combinations of antenna size and gate-oxide area consists of ten identical capacitors. Within a die there are $11 \times 2 \times 10 = 220$ capacitors. Each wafer consists of 84 die (actually 42 exposures of two duplicate patterns) giving a total of 18 480 test structures per wafer.

Damage is produced in the test structures by exposing the fully processed wafers to a plasma environment. The plasmas were generated in the ECR system using O_2 as the feed gas. In this situation, the primary role of the plasma is to provide a source of charged particles to the wafer surface.

The plasma-induced damage is assessed with ramp-voltage measurements of the test structures. The result of this measurement is a current-voltage (I–V) characteristic of the device under test. The I–V trace is obtained by applying a linear voltage ramp to the gate of the test structure and measuring the current flowing through the circuit. A typical voltage ramp rate is about one to two volts per second. Quantitative data obtained from the ramp-voltage technique include the capacitor breakdown voltage (V_{bd}) and leakage current ($I_{leakage}$). The breakdown voltage may be defined either as 1) the "run-away" voltage where the current increases by a factor of ten for a gate voltage increase of less than 0.1 V, or 2) the gate voltage when the current reaches 1 μA. The second definition, which is used in this work, is more commonly used in industrial applications because a transistor will definitely not work if this condition is reached at gate voltages relevant to normal device operation. The degree of damage for a processed test wafer was defined as the percentage of test structures with low (or "early") breakdown voltages below five volts.

C. Dual-Electrode Assembly

A diagram of the dual-electrode assembly which was used to modify the plasma uniformity is shown in Fig. 3. It consists of two separate electrodes (a solid ring and a circular grid) which are positioned over the wafer stage as shown. The ring was mounted 50 mm above the wafer stage and has an inner diameter of 98 mm and an outer diameter of 127 mm. The grid was mounted 50 mm above the ring and has a diameter of 45 mm. The grid material is 90% transparent and made from stainless-steel wire (0.13 mm in diameter) with a grid spacing (distance between adjacent grid wires) of 1.04 mm.

Two ceramic supports (50 mm in length) were used to electrically isolate the ring and grid from each other and from the wafer stage. Electrical isolation of the ring and grid electrodes with the ceramic supports is necessary so that the electrodes may be independently biased during operation. External connections are made to each electrode with insulated wires which are attached, at one end, to a BNC vacuum feedthrough, and, at the other end, to one of the electrodes.

III. Experimental Design

In order to investigate the effects of plasma-parameter variations on plasma-induced damage to MOS capacitor test structures, a two-step investigation was used. First the plasma nonuniformity generated by the dual-electrode assembly for various combinations of operating parameters was characterized. This consisted of 1) varying three parameters (pressure, grid bias, and ring bias) according to a three-factor two-level factorial design [20], 2) measuring radial profiles of the plasma parameters with a Langmuir probe; and 3) subsequently analyzing the probe data to characterize the spatial averages and standard deviations (nonuniformities) of the plasma parameters. In the second step, test wafers were exposed to the same combinations of settings investigated in the plasma-characterization step. Processing time was now

TABLE I
DESIGN TABLE FOR STEP I OF THE WAFER EXPOSURE EXPERIMENT. THE EXPERIMENTAL DESIGN IS A TWO-LEVEL THREE-FACTOR FULL FACTORIAL IN RANDOM RUN ORDER. RADIAL LANGMUIR PROBE SCANS WERE MEASURED FOR ALL OF THE POSSIBLE COMBINATIONS OF PRESSURE, GRID BIAS, AND RING BIAS LISTED ABOVE. IN ADDITION, THE MICROWAVE POWER WAS HELD FIXED AT 1000 W AND THE GAS FLOW RATE WAS ADJUSTED WITH THE PRESSURE AND WAS 14 SCCM FOR 0.5 MTORR AND 28 SCCM FOR 2.0 MTORR

Standard Order	Pressure (mTorr)	Grid Bias (Volts)	Ring Bias (Volts)
1	0.5	0	–25
2	2.0	0	–25
3	0.5	60	–25
4	2.0	60	–25
5	0.5	0	+25
6	2.0	0	+25
7	0.5	60	+25
8	2.0	60	+25

added as an additional factor, and the experimental design was thus a four-factor, two-level fractional factorial [20]. After processing, breakdown-voltage measurements of the test wafer were performed to determine the degree and location of the plasma-induced damage. The measurements of the plasma nonuniformity and the plasma-induced damage were then compared, and this analysis is described below after the results of both of the steps are presented.

The two-step process was needed because it was not possible to take probe measurements during exposure of the test wafers. A radial scan with the Langmuir probe took between five and ten minutes to complete, which is on the order of the processing time. Moving the probe across the test wafer on this time scale could greatly influence the damage results. To compensate for any process drift between the probe measurements and the wafer exposure, two radial profiles were measured, one before a wafer was processed and one afterwards. The results of the radial probe scans were then averaged to obtain values for the conditions during processing. Typically, the drift of the plasma parameters from before to after processing was less than five percent. Note that the plasma was shut off when a wafer was being transferred into and out of the system. In addition, during the wafer exposure, the Langmuir probe was withdrawn from the plasma.

The statistical experimental design for the characterization of the plasma nonuniformity (Step I) was a two-level three-factor full-factorial design with pressure, grid bias and ring bias as the factors. The design table for Step I is shown in Table I. The factor levels were 0.50 mTorr (low) and 2.00 mTorr (high) for pressure, 0 V (low) and 60 V (high) for grid bias, and -25 V (low) and $+25$ V (high) for ring bias. The microwave power was held constant and was set to 1000 W. The process gas was oxygen. In addition, the value of the gas flow rate was adjusted in combination with the pressure because of pumping-speed limitations, and was 14 sccm at 0.50 mTorr and 28 sccm at 2.0 mTorr. The radial scans with the Langmuir probe consisted of eleven measurements taken between $r = -5.00$ and $r = +5.00$ cm at intervals of 1.00 cm. In addition, the probe tip was positioned one centimeter above the surface of the wafer and the probe shaft was leveled horizontally so that the vertical separation between the probe tip and the wafer remained constant.

TABLE II
DESIGN TABLE FOR STEP II OF THE WAFER EXPOSURE EXPERIMENT. THE EXPERIMENTAL DESIGN IS A TWO-LEVEL FOUR-FACTOR FRACTIONAL FACTORIAL IN RANDOM RUN ORDER. TEST WAFERS CONTAINING THE MOS CAPACITOR ANTENNA TEST STRUCTURES WERE EXPOSED TO ALL OF THE COMBINATIONS OF PRESSURE, GRID BIAS, RING BIAS, AND PROCESSING TIME LISTED ABOVE. IN ADDITION, THE MICROWAVE POWER WAS HELD FIXED AT 1000 W, THE RF POWER APPLIED TO THE WAFER STAGE WAS SET AT 50 W, AND THE GAS FLOW RATE WAS ADJUSTED WITH THE PRESSURE AND WAS 14 SCCM FOR 0.5 MTORR AND 28 SCCM FOR 2.0 MTORR

Standard Order	Pressure (mTorr)	Grid Bias (Volts)	Ring Bias (Volts)	Process Time (min.)
1	0.5	0	–25	4
2	2.0	0	–25	8
3	0.5	60	–25	8
4	2.0	60	–25	4
5	0.5	0	+25	8
6	2.0	0	+25	4
7	0.5	60	+25	4
8	2.0	60	+25	8

During wafer exposure (Step II), processing time was added as a fourth experimental factor in addition to pressure, grid bias and ring bias. The factor levels for the processing time were 4 and 8 min. A full factorial design, using the four factors at two levels, would have required 16 runs. However, to keep the number of wafers consumed at a manageable level, only one half of the possible combinations of different factor levels was used. The actual combinations used were chosen according to a fractional-factorial procedure in which the level of the fourth variable (processing time) was determined by the levels of the three other factors [20]. The design table for Step II is shown in Table II. All of the other system parameters (power, gas flow rates, magnetic field configuration, etc.) were the same as in Step I, except for the rf power applied to the wafer stage, which was set at 50 W during the wafer exposures.

IV. RESULTS AND DISCUSSION

A. Plasma-Parameter and Breakdown-Voltage Measurements

Radial profiles of the plasma parameters (plasma and floating potentials, electron temperature, and plasma density) were generated and characterized in terms of their averages and standard deviations. Both the standard deviation and the data range (maximum minus minimum) could be used as a measure of the profile nonuniformity. Empirically, we have observed that the ratio of the standard deviation to the data range varies in the same manner and therefore these two quantities provide essentially the same information about the nonuniformity of the plasma-parameter profiles. We have used the standard deviation of the profile to gauge the nonuniformity because it takes into account all of the data from a profile and is thus less sensitive to abnormally high or low observations (noise).

The averages and nonuniformities of the plasma parameters measured at the different experimental combinations varied over a wide range. Extreme cases (the most uniform and most nonuniform examples) of the plasma-potential, floating-

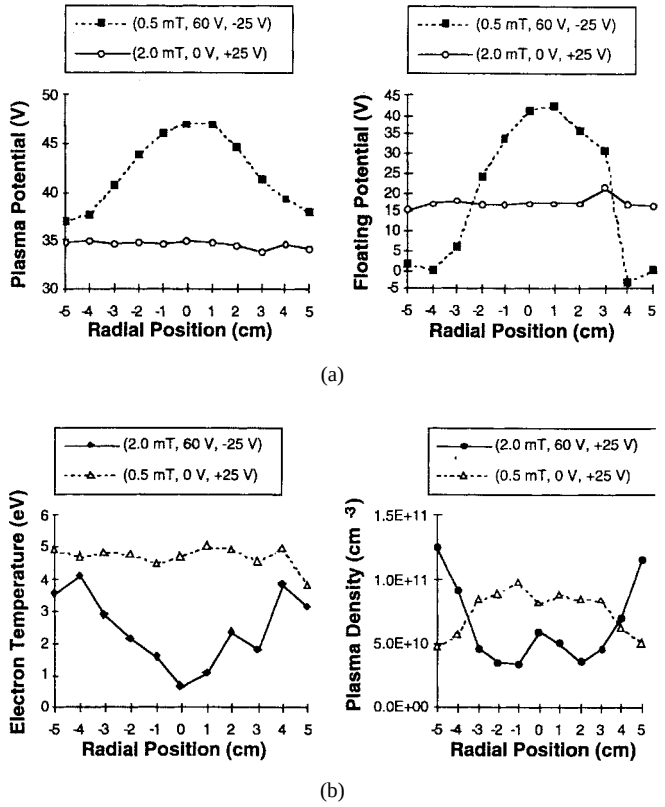

Fig. 4. Extreme cases of (a) plasma-potential, (b) floating-potential, (c) electron-temperature, and (d) plasma-density nonuniformity generated with the dual-electrode assembly during Step I of the wafer-exposure experiments. The processing conditions (pressure, grid bias, and ring bias) for the dual-electrode assembly for each condition are indicated in each figure.

potential, electron-temperature, and plasma-density profiles can be seen in Fig. 4(a)–(d), respectively. The standard deviation of the plasma-potential profiles ranged from 0.20–3.9 V, while the average of the plasma-potential profile data ranged from 12.1–58.6 V. The extreme values of the averages and standard deviations for the other plasma parameters are given in Table III. Note that, in general, the average and standard deviation for each parameter are not strongly correlated; a high profile average does not imply that the profile nonuniformity is large (and vice versa).

A detailed discussion of the relationship between the experimental factors (ECR system pressure and electrode biases) and the radial profiles of the plasma parameters is provided by Friedmann [21]. Some of the most important effects include: 1) an inverse relationship between the pressure and the electron temperature based on the need to maintain the balance between the rates of ion creation and loss in steady state [22]; 2) an increase in the average plasma potential in response to increases in the electrode biases in order to reach a steady state limit for the loss of electrons to the other plasma boundaries; 3) a decrease in the plasma density below the grid as the grid bias is increased and the electron current collected by the grid increases, and iv) an increase in the nonuniformity of the plasma-potential profiles as the potential difference between the grid and ring electrodes increases. The nonuniformity in the plasma potential is set up because of the different potentials

TABLE III
CORRELATION COEFFICIENTS BETWEEN THE EARLY BREAKDOWN PERCENTAGES AND (a) THE NONUNIFORMITIES OF THE PLASMA-PARAMETER PROFILES; (b) THE SPATIAL AVERAGES OF THE PLASMA-PARAMETERS

Nonuniformity of Profiles	Minimum	Maximum
Plasma Potential	0.20 V	3.9 V
Floating Potential	1.5 V	18.4 V
Electron Temperature	0.25 eV	1.4 eV
Plasma Density	$1.7\text{x}10^{10}$ cm^{-3}	$3.2\text{x}10^{10}$ cm^{-3}

(a)

Profile Average	Minimum	Maximum
Plasma Potential	12.1 V	58.6 V
Floating Potential	-7.5 V	28.1 V
Electron Temperature	2.6 eV	6.4 eV
Plasma Density	$2.5\text{x}10^{10}$ cm^{-3}	$1.9\text{x}10^{11}$ cm^{-3}

(b)

(and resulting radial electric field) between magnetic field lines that are in contact with the ring electrode and field lines that are in contact with the grid.

The processed test wafers, which were exposed to the same conditions for which the Langmuir probe data was obtained, were characterized with breakdown-voltage measurements and cumulative-percentage plots of the breakdown voltage to determine the early breakdown percentage (as described above). For the test structures with the largest field-oxide area ($80 \times 5000\,\mu\text{m}^2$) which should show damage first, the extreme levels of damage observed from the wafer exposures were 0 and 39%. In terms of operating conditions, the minimum damage was observed at a pressure of 2.0 mTorr, a grid bias of 0 V, a ring bias of -25 V, and a processing time of 4 min. The operating conditions at which the maximum damage level occurred were a pressure of 0.5 mTorr, a grid bias of 60 V, a ring bias of -25 V, and a processing time of 8 min. Plots of the cumulative percentage of the breakdown voltages of the test structures with the largest antenna ratios from these two different wafer exposures are shown in Fig. 5.

B. Statistical Correlations Between Damage Data and Plasma Measurements

Statistical correlation coefficients between the spatial averages and standard deviations of the plasma-parameter profiles and the early breakdown percentages have been calculated and are listed in Table IV. The largest correlation coefficients (approximately 0.9) are between the early breakdown percentage and both the plasma-potential and the floating-potential nonuniformity. These are strong positive correlations which suggest that the early breakdown damage is greater when the plasma-potential and/or floating-potential nonuniformities are greater. The correlations with the remaining nonuniformities are almost as strong as the correlation with the plasma-potential nonuniformity.

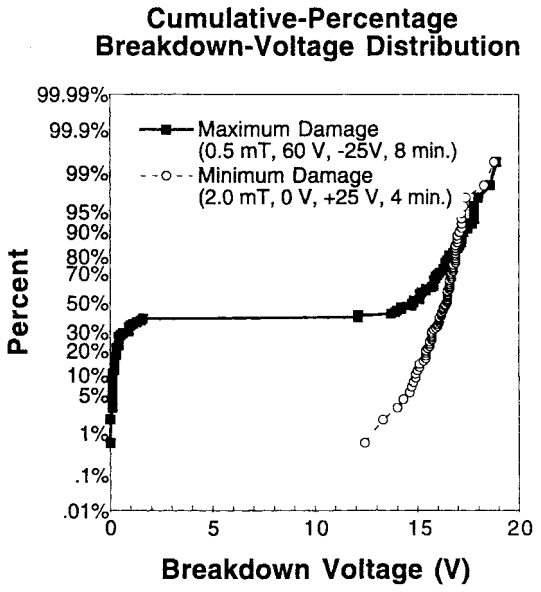

Fig. 5. Cumulative-percentage breakdown-voltage distributions of the test wafers from Step II of the wafer-exposure experiment which showed the minimum and maximum levels of damage. The processing conditions for the wafers are indicated in the legend.

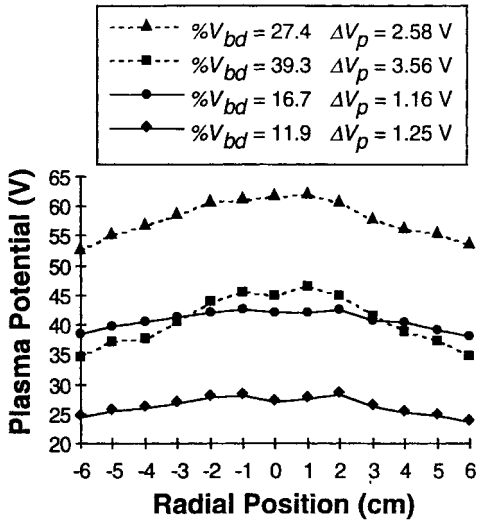

Fig. 6. The plasma-potential profiles measured when the grid bias was set at 60 V are shown. The early breakdown percentages for wafers exposed to these conditions and the calculated standard deviation of the profiles are shown in the legend. As can be seen, the damage scales with the plasma-potential nonuniformity of the profiles and not with the average plasma potential.

TABLE IV
MINIMUM AND MAXIMUM VALUES OF THE NONUNIFORMITY (a) AND AVERAGES (b) OF THE PLASMA-PARAMETER PROFILES GENERATED BY THE DUAL-ELECTRODE ASSEMBLY. THE DATA WAS MEASURED DURING STEP I OF THE WAFER-EXPOSURE EXPERIMENT

Plasma Parameter	Correlation Coefficient between Spatial Average of Plasma-Parameter Profile and Early Breakdown Percentage
Plasma Potential	0.39
Electron Temperature	0.67
Plasma Density	–0.60
Floating Potential	0.46

(a)

PlasmaParameter	Correlation Coefficient between Nonuniformity of Plasma-Parameter Profile and Early Breakdown Percentage
Plasma Potential	0.93
Electron Temperature	0.80
Plasma Density	–0.73
Floating Potential	0.88

(b)

The smallest correlation coefficient (0.39) is between the early breakdown percentage and the average plasma potential. That the early breakdown damage is more strongly related to the nonuniformity of the plasma-potential profiles than to the spatial average of the plasma-potential profiles can be demonstrated graphically, as shown in Fig. 6. In this plot the four plasma-potential profiles taken with a grid bias of 60 V are shown. These profiles were chosen because the largest degree of early breakdown damage and plasma-potential nonuniformity were observed when the grid was set at the 60 V level. The averages of the plasma-potential profiles are evident from their location along the voltage (vertical) axis of the plots. The standard deviations of the profiles (ΔV_p) as well as the early breakdown percentages (%V_{bd}) of the test wafers exposed to these conditions are indicated at the top of Fig. 6. As can be seen, the damage level correlates with the plasma-potential nonuniformity and not with the average of the plasma-potential profile. This observation is also valid for the floating potential profiles.

C. Variation of Charging Conditions Across the Wafer Surface

Charge build-up on the gates of the MOS capacitor test structures produces potential differences across the gate oxide that result in F–N tunneling current flow through that gate-oxide layer. This current degrades the quality of the oxide and can eventually lead to dielectric breakdown [23]. In a plasma environment, this charge build-up may be caused by local differences in the ion and electron currents to the individual gates of the test strucutres [24]. To see if the damage observed in our experiments can be explained in this manner, we will investigate the charging that exists across the surface of the wafer during processing, so as to determine whether there are locations on the wafer where charging damage could occur.

One indication of how the local charging conditions are changing is provided by examination of the floating-potential profiles generated from the Langmuir probe measurements. By definition, the floating potential is the potential at which the ion and electron currents to the probe are balanced. Therefore, the floating potential will vary in response to changes in these two current components. The values of the ion and electron currents to the Langmuir probe are functions of the local plasma density and the electron temperature. The electron current also depends on the ratio of the difference between the plasma potential (V_p) and the probe bias (V_B) to the electron temperature (T_e), $(V_p - V_f)/T_e$. This ratio determines

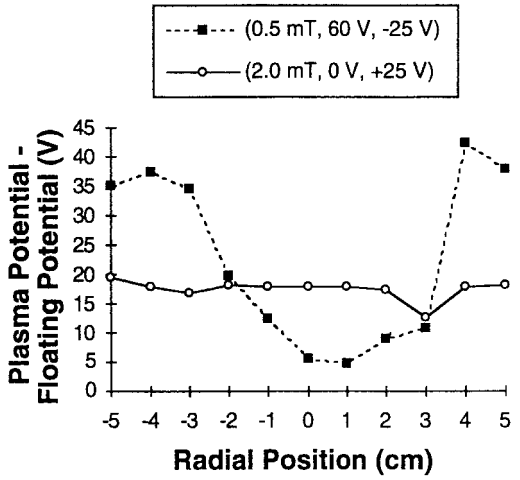

Fig. 7. The difference between the plasma potential and the floating potential for the profiles plotted previously in Fig. 4 are shown. For the uniform profile, the difference between the two potentials remains relatively constant. The nonuniform profile shows that the floating potential is much closer to the plasma potential in the center of the plasma and indicates that the floating potential is not simply following the changes in the plasma potential. The processing conditions are provided in the figure.

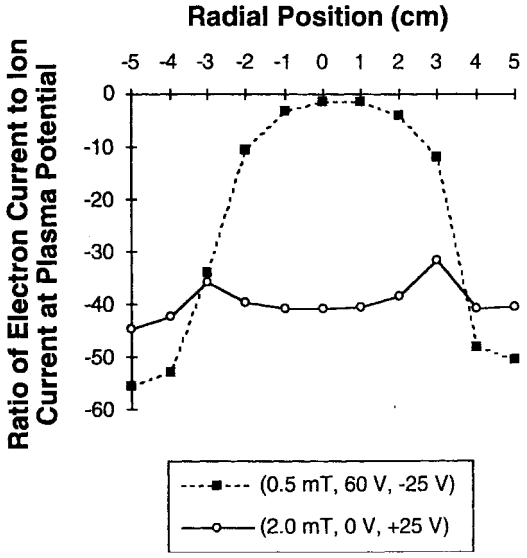

Fig. 8. Ratio of the electron current to the ion current at the plasma potential as determined from the Langmuir probe measurements. The processing conditions for the uniform and nonuniform profiles are the same as those in Figs. 4 and 7.

the fraction of electrons in the plasma which have sufficient kinetic energy to overcome the potential-energy barrier at the probe, according to the Boltzmann relationship [25]. This means that the floating potential is ultimately adjusted by the changes in the local plasma conditions (plasma potential, electron temperature, and ion and electron densities).

As was shown in Fig. 4(b), the floating-potential profiles generated when the dual-electrode assembly is used exhibit a wide range of spatial averages and nonuniformities. In this figure, the uniform profile is relatively flat, with an average of 17.1 V and a standard deviation of 1.5 V, while the average and standard deviation of the nonuniform floating-potential profile are 19.3 and 18.4 V, respectively.

It may be possible that the changes in the floating-potential profiles simply reflect the variation of the plasma potential across the surface of the wafer. To see that this is not the case, we can reference the floating potential to the plasma potential and plot radial profiles of the difference between them. (If the floating potential were following the plasma-potential variations, we would expect that their difference would be constant.) Profiles of the difference between the plasma-potential and floating-potential profiles ($V_p - V_f$ profiles) plotted in Fig. 4(b) are shown in Fig. 7. Looking at the $V_p - V_f$ profiles in Fig. 7, we can see that, in the uniform case, the difference between the plasma potential and the floating potential is relatively constant across the surface of the wafer (about 17.5 V). For the most nonuniform case, however, the potential difference ranges from 4.8–42.4 V. Therefore, the floating potential is not following the variations of the plasma potential. In particular, for nonuniform profiles we see that the floating potential is closer to the plasma potential near the center of the wafer.

As mentioned above, the floating potential varies in response to changes in the local values of the plasma potential, electron temperature, and ion and electron densities, in order to satisfy the floating condition (net current equal to zero). When a Langmuir probe is biased at the plasma potential, however, the ion and electron currents collected by the probe are unequal. In an unmagnetized dc plasma, the ratio of the electron saturation current to the ion saturation current is given by the square root of the ratio of the electron mass to the ion mass [26]. For an oxygen plasma, this ratio is 242. In a magnetic field, the electron current to a probe is suppressed because electrons are held tightly to the magnetic field lines and their mobility across the magnetic field is limited [27]. In this ECR system, which has a strong magnetic field, the measured saturation current ratio is typically about 50. As the ratio of the electron current to the ion current at the plasma potential changes, the floating potential will be different. For example, assuming the other plasma parameters remain constant, if the current ratio decreases (either due to a decrease in the electron current or an increase in the ion current) the floating potential will increase toward the plasma potential since the potential difference needed to achieve current equalization is smaller.

Radial profiles of the ratios of the electron current to the ion current at the plasma potential (I_e/I_i profiles) for the two cases shown in Fig. 7 are plotted in Fig. 8. For the uniform I_e/I_i profile shown in Fig. 8, the current ratio ranges from -32 to -45, and for the nonuniform profile the range of the ratio is from -1.4 to -55. The uniformity of the current-ratio profiles is determined mainly by the level of the grid bias, being more nonuniform when the grid bias is high. As can be seen, the $V_p - V_f$ profiles (Fig. 7) follow the variation of the current-ratio profiles. The variations in the plasma potential and the electron temperature will also affect the value of the local floating potential, but the changes resulting from the different current ratios are seen to dominate the behavior of the floating-potential profiles.

The electron and ion currents, from which the ratios plotted in Fig. 8 were calculated, are shown in Fig. 9(a) and (b),

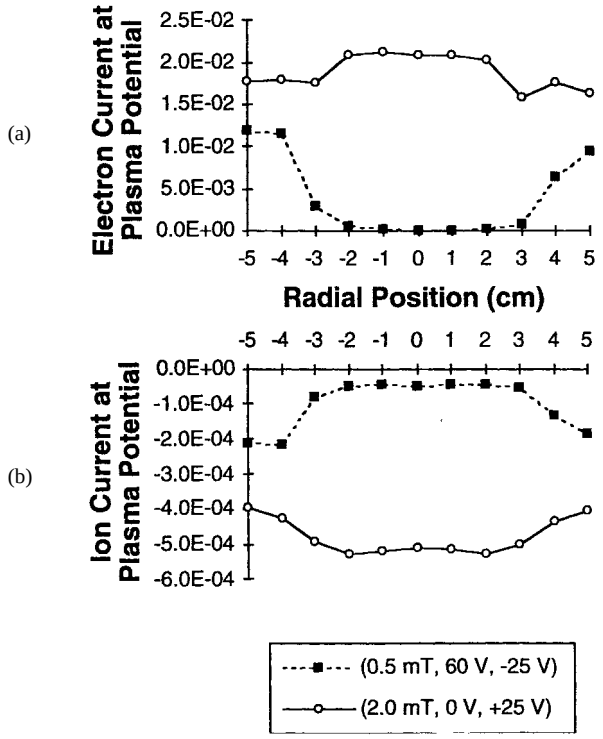

Fig. 9. (a) The electron current and (b) the ion current for the nonuniform (NU) and uniform (U) profiles shown in Fig. 8.

respectively. Based on these Figures we can see that, in the nonuniform case, the variation in the current ratio is primarily due to the decrease in the electron current beneath the grid compared to the ion current. In the nonuniform case, the electron current is over 100 times greater at the edge of the wafer relative to the center, while the ion current is only about four times greater at the edge of the wafer in comparison to the center. The greater reduction of the electron current in the center of the wafer (in proportion to the wafer edge) at high grid bias is due in part to a depletion of electrons along the magnetic field lines that are connected to the grid electrode and more effective cross-field diffusion of ions compared to electrons [21].

To relate the above discussion to the wafer charging conditions, we must consider what is occurring on the surface of the wafer. Initially, before any of the antenna structures have broken down, the test wafer behaves as an insulator. This implies that the wafer must locally satisfy the floating condition and currents cannot flow along the wafer surface. When the plasma is turned on, the ion and electron currents to the wafer surface (and the other plasma boundaries as well) are unbalanced. Specifically, the electron current is initially much greater than the ion current because of the differences in their mobilities. Since the wafer is an insulator, charge will build up due to the local imbalance of the ion and electron currents. This surface charge changes the potential of the wafer with respect to the plasma, which in turn causes the electron current to adjust. Eventually, sufficient charge accumulates and a steady state is reached [24] in which either 1) the ion and electron currents are balanced, or 2) a current is flowing through the gate oxide of the test structure

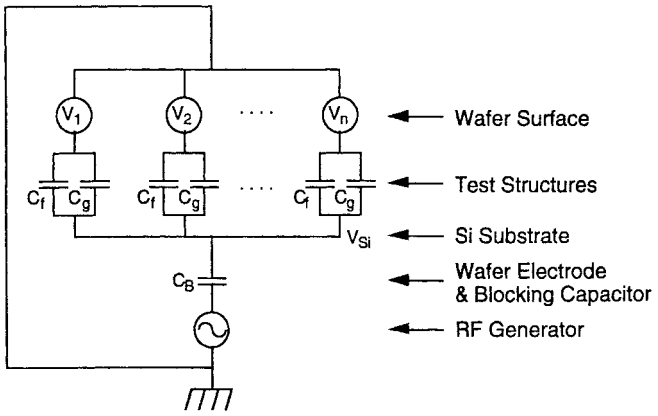

Fig. 10. Equivalent-circuit model of the test wafer and the wafer-stage electrode. The individual test structures are represented as the parallel network of the field-oxide capacitor C_f and the gate-oxide capacitor C_g. Each test structure is allowed to have a different gate voltage (V_i, $i = 1$ to n, where n is the number of test structures) to account for variations in the floating potential across the surface of the wafer. The wafer-stage electrode, the rf blocking capacitor, and the tuning capacitors in the matching network are represented by the series capacitance C_B.

which accounts for the difference in the local ion and electron currents.

Because the plasma parameters are varying over the wafer, the amount of surface charge (and hence the floating potential) will also vary. However, since an rf self bias was applied to the wafer electrode during processing, we must consider how this affects the substrate charging.

When an rf signal is capacitively coupled to a substrate as shown in Fig. 10, an rf self-bias will develop across the coupling capacitor so that the total charge flow per cycle equals zero [25]. That is, the average value of the rf voltage shifts toward a negative potential so that the ion and electron currents to the substrate sum to zero over each rf cycle. The average value of the rf voltage shifts toward negative potential because of the greater mobility of electrons compared to ions, which implies that, in order to conduct a given current, a much smaller potential is required for electrons than for ions [25].

Typically, the magnitude of the rf self-bias is equal to about half of the peak-to-peak rf voltage. For a fixed level of power, the peak-to-peak rf voltage is smaller (and hence the self-bias is less negative) when the plasma density is larger. Conversely, the self-bias shifts toward a negative potential when the plasma density decreases. Given the configuration of the wafer chuck in the ECR system, it was not possible to make measurements of the rf self bias of the wafer. Because the rf power is capacitively coupled to the substrate and the surface of the electrode is an insulator, a dc electrical connection cannot be made. However, measurements have been made in the ECR system by other researchers using an alternative electrode configuration [28]. Their results show that for an rf power level of 50 W, the rf self bias ranges between -25 to -75 V depending on the system conditions. When the rf signal is applied, the rf self bias appears across the coupling capacitor, causing the potential on the surface of the wafer to shift in the direction of the self-bias potential. However, because of the variation of the ion and electron currents across the wafer surface, nonuniform charging will still occur. In particular,

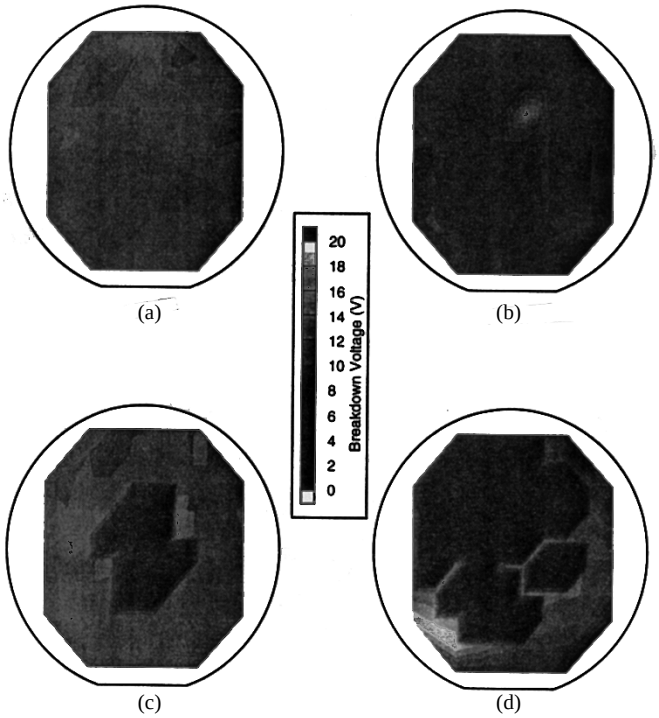

Fig. 11. Wafer maps of the breakdown voltages for test wafers which exhibited (a) the lowest level of damage (0%), (b) the next lowest level of damage (2%), (c) the third lowest level of damage, and (d) the maximum level of damage. The conditions (pressure, grid bias, ring bias, and time) were: (a) (2.0 mTorr, 0 V, −25 V, 8 min), (b) (0.5 mTorr, 0 V, − 25V, and 4 min), (c) 2.0 mTorr, 60 V, −25 V, and 4 min), and (d) (0.5 mTorr, 60 V, −25 V, and 8 min).

given the current-ratio nonuniformities shown in Fig. 8, the wafer will charge more positively at its center.

D. Pre-Breakdown Equivalent-Circuit Model

The silicon substrate of the wafer has a low resistivity and can be considered an equipotential. In order to determine the potential of the silicon substrate with respect to the potential on the surface of the wafer, consider the equivalent circuit of the test wafer and the electrode shown in Fig. 10. Each test structure is represented as a pair of capacitors, C_f and C_g, connected in parallel. C_f and C_g vary depending on the thickness of the field and gate oxides and the size of the polysilicon pad. In addition, V_{Si} is the potential of the silicon substrate with respect to ground and C_B represents the series capacitance of 1) the gap between the wafer and surface of the electrode, 2) the anodized aluminum layer on the surface of the electrode, 3) the rf blocking capacitor itself, and iv) the tuning capacitors of the rf matching network. Henceforth, we will refer to this series combination as the blocking capacitor.

When an rf signal is applied to the wafer stage through the blocking capacitor, an rf self bias appears. Bias charges appear both across the blocking capacitor C_B, as well as across the individual test structures. We let the bias charge on the blocking capacitor be Q_B, and the bias charge on each individual test structures be Q_i (where $i = 1, \cdots, n$, and n is the number of test structures). Because the blocking capacitor C_B is connected in series with each test structure, the charge on the blocking capacitor (Q_B) must equal the sum of the charges on the individual test structures ($Q_1, Q_2, \cdots, Q_n$). That is, for the n test structures,

$$Q_B = Q_1 + Q_2 + \cdots + Q_n. \tag{1}$$

In addition to the self-bias charge, floating potential variations across the surface of the wafer will result in additional charge flowing into these capacitors. Referring to Fig. 10, each test structure has a specific floating potential feeding charge to it. We represent these floating potentials as an array of voltage sources. The voltage source feeding test structure i has a value V_i which causes the charge ΔQ_i to flow into that particular test structure as well as into C_B. Since the capacitor C_B is connected in series with each test structure, the net charge ΔQ_B that accumulates in C_B is the sum of the additional charges on all of the individual test structures. Therefore, similarly to (1), we write

$$\Delta Q_B = \Delta Q_1 + \Delta Q_2 + \cdots + \Delta Q_n. \tag{2}$$

Using Kirchoff's voltage law, we now sum the voltages around each loop of the circuit to yield

$$\begin{aligned} V_1 &= \frac{Q_1 + \Delta Q_1}{C_f + C_g} + V_{Si}, \\ V_2 &= \frac{Q_2 + \Delta Q_2}{C_f + C_g} + V_{Si}, \\ &\vdots \qquad\quad \vdots \\ V_n &= \frac{Q_n + \Delta Q_n}{C_f + C_g} + V_{Si}. \end{aligned} \tag{3}$$

We let C represent the average parallel capacitance of each test structure ($C = C_f + C_g$) and sum these n equations to get

$$\begin{aligned} V_1 + V_2 + \cdots + V_n = &\frac{Q_1 + \Delta Q_1}{C} + \frac{Q_2 + \Delta Q_2}{C} + \cdots \\ &+ \frac{Q_n + \Delta Q_n}{C} + nV_{Si} \end{aligned} \tag{4}$$

or

$$\sum_{i=1}^{n} V_i = \left[\frac{\sum_{i=1}^{n} (Q_i + \Delta Q_i)}{C} \right] + nV_{Si}. \tag{5}$$

Substituting (1) and (2) gives

$$\sum_{i=1}^{n} V_i = \frac{Q_B + \Delta Q_B}{C} + nV_{Si}. \tag{6}$$

But, since $Q_B + \Delta Q_B = C_B V_{Si}$

$$\sum_{i=1}^{n} V_i = \frac{C_B V_{Si}}{C} + nV_{Si} = \left(\frac{C_B}{C} + n \right) V_{Si}. \tag{7}$$

Dividing both sides by the expression enclosed in parentheses yields the following expression for the potential of the silicon substrate:

$$V_{Si} = \frac{\sum_{i=1}^{n} V_i}{\frac{C_B}{C} + n}. \tag{8}$$

In effect, (8) shows that V_{Si} is produced as the result of a series capacitive voltage-dividing action between capacitors C_B and nC. That is, the two capacitors of the series voltage divider are 1) the series capacitance of the wafer electrode and rf network and 2) the parallel capacitance of the n MOS capacitor test structures.

Approximating the capacitors of the test structures as parallel plate capacitors, the average capacitance C of an antenna structure is calculated to be 10 pF using a relative dielectric constant for SiO_2 of 3.9. As described above, the capacitance C_B includes the series capacitances of the wafer-electrode gap, the anodized aluminum layer on the surface of the wafer electrode, the rf blocking capacitor, and the tuning capacitors of the rf matching network. The capacitance of this series network is approximately 1 nF. Therefore, the ratio C_B/C in (8) is $\approx$100. By comparison, the number of test structures on a wafer (n) is on the order of 20 000. Consequently, we can neglect the capacitance ratio C_B/C compared to n in the denominator of (8), so it becomes

$$V_{Si} = \frac{1}{n} \sum_{i=1}^{n} V_i. \tag{9}$$

The potential of the silicon substrate is thus the average potential on the gates of the test structures. Since the test structures are located uniformly across the surface of the wafer, we can approximate the potential of the silicon substrate as the average potential across the surface of the wafer.

If the potential across the surface of the wafer is uniform, the potential of the silicon substrate will be equal to the potential on the surface of the wafer, and the potential difference across the gate-oxide layers of the test structures will be small. If, on the other hand, the potential across the surface of the wafer is nonuniform, the potential of the silicon substrate will be between the extremes of the surface potential. In this case, large potential differences can occur across the gate-oxide layers of the test structures depending on the shape and magnitude of the nonuniformity. When the magnitude of these potential differences between the gate of the test structures and the silicon substrate is large enough, F–N current will tunnel through the gate-oxide layer and create damage. Profiles of the potential difference across the gate-oxide layer have been calculated and will be presented in the following section.

It should be noted that this model and its calculations are based on the situation that exists before Fowler–Nordheim tunneling happens. Since the damage is actually caused by the tunneling current, once tunneling occurs the voltage V_i will change according to the local plasma current drive capacity after tunneling.

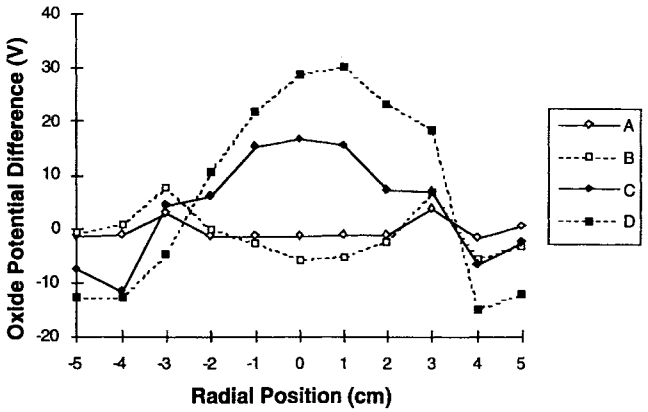

Fig. 12. The calculated profiles of the potential difference across the gate-oxide layer. These profiles correspond to the wafer maps shown in Fig. 11.

E. Whole-Wafer Maps of Plasma-Induced Damage

Whole-wafer maps of the breakdown-voltage data for the test structures with the largest antenna ratios have been made. These maps show where the damage is occurring on the test wafers. The wafer maps measured for the wafer exposed to conditions in which the ring bias was set at -25 V are shown in Fig. 11(a)–(d), which are ordered in terms of increasing damage levels. (Note that the wafers exposed to conditions in which the ring bias was set at $+25$ V, but with the same levels for pressure and grid bias, exhibited similar damage levels.) The wafer maps with the minimum (0%) and maximum (39%) damage levels are shown in Fig. 11(a) and (d), respectively. The map for the minimum damage level shows only small variations in the breakdown voltage between 13–16 V. These variations are characteristic of the intrinsic breakdown of the test structures and, in this case, none of the test structures displayed early breakdown. The breakdown voltages on the map of the wafer with the maximum damage range from 0–18 V, and there are both large areas where the test structures have experienced significant early breakdown and areas where the test structures appear to be undamaged.

Assuming that the variation of the wafer surface potential during processing is the same as the variation of the floating-potential profiles measured with the Langmuir probe, we can use the results of the equivalent-circuit model presented in the previous section to calculate radial profiles of the potential difference across the gate-oxide layers. First, the potential of the silicon substrate is calculated as the area-weighted average of a particular floating-potential profile assuming azimuthal symmetry. The oxide potential-difference profiles are then generated by subtracting the silicon-substrate potential from the individual floating-potential measurements of the profile. The oxide potential-difference profiles for the wafer maps from Fig. 11 are shown in Fig. 12. In relationship to the two-dimensional wafer maps, the Langmuir-probe profiles were measured along a line rotated approximately 75° counterclockwise from the diameter that is parallel to the major flat of the wafer.

Comparing the wafer maps and the potential-difference profiles, it is evident that the damaged regions correspond to

the locations where the potential difference across the gate-oxide layer is largest. For the wafer map shown in Fig. 11(a), the calculated potential difference (profile A in Fig. 12) ranges from -3 V to $+4$ V. The F–N tunneling current that can flow through the gate oxide under the influence of this potential difference can be determined from the Fowler–Nordheim current equation [29], [30], which is the current-voltage characteristic for F–N tunneling:

$$I_{F-N} = A_g C \left(\frac{V_{ox}}{t_g}\right)^2 \exp\left(\frac{-\alpha t_g}{V_{ox}}\right). \tag{10}$$

Here, I_{F-N} is the F–N tunneling current flowing through the test structure and V_{ox} is the potential across the thin gate oxide. A_g is the area of the thin gate oxide through which the current is flowing and t_g is the thickness of the thin gate oxide layer as described above. In addition, $C = 20\,\mu$A/V^2, and $\alpha = 250$ MV/cm are known constants [30]. Note that (10) assumes that the current density is uniform across the gate oxide area of the test structure. Using the largest potential difference (4.1 V) shown in profile A of Fig. 12, the F–N current through a single MOS capacitor test structure with a gate-oxide area of 400 μm^2 and a gate-oxide thickness of 10 nm is calculated to be 9.2×10^{-25} A. Clearly, the gate oxide will not be damaged under these conditions.

For Fig. 11(b), the corresponding potential difference profile (profile B in Fig. 12) ranges from -6–9 V, and is peaked at $r = \pm 3$ cm. Examining the wafer map for this profile [Fig. 11(b)], we can see that a low level of damage is evident near the same radial locations as the potential-difference peaks. For a gate-oxide potential difference of 9 V, the F–N tunneling current is 5.6×10^{-9} A, which is small. However, since the azimuthal locations of the probe measurements and the regions of damage are not the same, it is likely that asymmetries exist such that the oxide potential difference is larger in the damaged regions.

The wafer maps of the breakdown voltages shown in 11(c) and (d) exhibited the largest damage levels. These wafers were exposed when a high bias (60 V) was applied to the grid of the dual-electrode assembly, which were the same processing conditions which generated the largest nonuniformities of the plasma parameters. The wafer map of Fig. 11(c) shows that the majority of the damage is occurring near the center of the wafer where the calculated oxide potential differences are the greatest. For these conditions the oxide potential difference were between -11 and 16 V. For the -11 V potential difference, the F–N tunneling current is 1.3×10^{-6} A, which is beginning to approach a level at which breakdown voltage degradation can occur. For the 16 V potential difference, the F–N tunneling current is calculated to be 3.4×10^{-3} A. When the F–N current is of this magnitude, breakdown of the gate-oxide layer will quickly occur. For the wafer maps shown in Fig. 11(d), the calculated profiles of the oxide potential difference (profile D in Fig. 12), as well as the overall damage levels, are greater than those shown in Fig. 11(c) and profile C in Fig. 12. Here, the potential differences ranged from -15–30 V with correspondingly large F–N tunneling currents. In addition, damage is evident both at the center and edges of the wafer, consistent with the profiles of the oxide potential difference.

V. Summary and Conclusions

In studying plasma-induced damage in the ECR system, the dual-electrode assembly was used to controllably adjust the absolute magnitude and nonuniformity of the plasma parameters. After being subjected to these varied plasma conditions, the test wafers exhibited a wide range of damage levels as well.

Statistical correlations between the spatial averages and nonuniformities of the plasma-parameter profiles and the early breakdown percentages showed that the nonuniformities of both the plasma potential and the floating potential are most strongly correlated with the degree of plasma-induced damage. Strong correlations also exist between the early breakdown percentage and the nonuniformity of both the electron-temperature and plasma-density profiles. In addition, the correlations show that the averages of the plasma-potential and floating-potential profiles are not determining factors for generating damage.

The variation of the floating-potential profiles is evidence of the variation of the ion and electron currents across the surface of the wafer. In particular, the floating potential is larger in the center of the plasma when the grid bias of the dual-electrode assembly is set at a high level because the electron current is suppressed (or depleted) underneath the grid in comparison to the ion current. Since the wafer is (initially) an insulator, the surface must locally satisfy the floating condition Thus, the floating potential provides an indication of the degree of local surface charging.

From the equivalent-circuit model of the test wafer and the wafer-stage electrode it was determined that the potential of the silicon substrate is approximately equal to the average potential across the surface of the wafer. Therefore, when the potential across the surface of the wafer is uniform, the potential of the silicon substrate will be equal to the potential on the surface of the wafer, and the potential difference across the gate-oxide layers of the test structures will be small. When the potential across the surface of the wafer is nonuniform, the potential of the silicon substrate is located between the extremes of the surface potential. In this case, large potential differences can occur across the gate-oxide layers of the test structures depending on the shape and magnitude of the nonuniformity.

When the magnitude of the potential differences between the gates of the test structures and the silicon substrate is large enough, F–N current will tunnel through the gate-oxide layer and create damage. Radial profiles of the potential differences between the surface of the wafer and the silicon substrate were calculated by assuming that the variation of the initial wafer surface potential is equal to the variation of the floating potential measured with the Langmuir probe. The calculated potential differences were largest when the plasma was most nonuniform. In addition, whole wafer maps of the breakdown voltages indicate that the majority of the damage is occurring in the regions where the potential differences across the gate

oxide are large. From the wafer maps, the damage is seen to be complete in localized regions. Since the damage occurs nonsymmetrically, the region of the wafer on which large potential differences (and hence the greatest amount of local charging) are developed is most likely determining the overall damage levels of the entire wafer.

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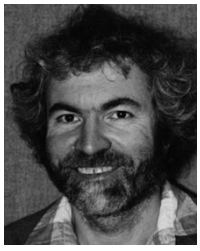
He is currently working for Texas Instruments Semiconductor Group in the DP1 wafer fab, Dallas, TX. This work includes development and production of polysilicon and silicon etch processes for 0.25 and sub-0.25 μm geometries.

J. Leon Shohet (S'56–M'62–SM'72–F'78) received the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA, in electrical engineering in 1961.

He served on the faculty of The Johns Hopkins University, Baltimore, MD, before joining the faculty of the University of Wisconsin, Madsion, in 1966, where he was appointed Professor of Electrical & Computer Engineering in 1971. He currently serves as the Director of the University's NSF Engineering Research Center for Plasma-Aided Manufacturing as well as the Director of the Torsatron/Stellarator Laboratory, a major Department of Energy fusion research facility, and is the past Chairman of the Department of Electrical and Computer Engineering. He is the author of two textbooks on plasma science, more than 125 journal articles, and more than 400 conference papers. He holds six patents. His research interests are: plasma-aided manufacturing; fusion, especially waves, instabilities, heating, confinement, and diagnostics; communications; magnetohydrodynamics; electromagnetic field theory; biophysics; quantum electronics, and lasers.

Dr. Shohet is a Fellow of the American Physical Society. He received the Frederick Emmons Terman Award of the American Society for Engineering Education, the Merit Award of the IEEE's Nuclear and Plasma Sciences Society, the IEEE Richard F. Shea Award, the IEEE Plasma Science Prize, the IEEE Centennial Medal, and the John Yarwood Memorial Medal from the British Vacuum Council. He founded the IEEE TRANSACTIONS ON PLASMA SCIENCE in 1973.



Robert Mau recently receved the Ph.D. degree in statistics, with a minor in art history, from the University of Wisconsin, Madison under Michael Newton. His dissertation was the application of MCMC to phylogenetic inference, which he has presented to the statistics and evolutionists community.

He has been collaborating with scientists at the ERC for the last three years, and hopes to pursue a career in industry.

Dr. Mau was a winner of the student paper competition sponsored by the statistical computing section of the American Statistical Association.

Noah Hershkowitz (SM'82–F'89) was born in Brooklyn, NY, on August 16, 1941. He received the B.S. degree in physics from Union College, Schenectady, NY, and the Ph.D. degree from the Johns Hopkins University, Baltimore, MD, in 1966.

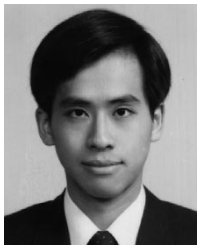
He worked as an Instructor at The Johns Hopkins University until he joined the University of Iowa, Iowa City, as an Assistant Professor in 1967. From 1967 to 1971, he carried out Mössbauer effect studies of nuclear physics and magnetism, and from 1971 to 1981 he worked with experimental basic plasma physics. During leaves from the University of Iowa, he spent 1974 to 1975 and 1980 to 1981 at the University of California, Los Angeles, and the University of Colorado, Boulder. Since 1981, he has been Professor of Nuclear Engineering and Engineering Physics and Director of the Phaedrus Laboratory for Plasma Science at the University of Wisconsin, Madison. He has held the position of Irving Langmuir Professor at this institution since 1987. His current research is a combination of basic plasma physics and plasma processing. He is a widely recognized expert in areas that include ion acoustic solutions, electrostatic shocks, double layers, plasma sheaths, emissive probes, electrostatic confinement in tandem mirrors, and ponderomotive force from ICRF. His most recent interest has been directed to ICRF current drive (near and below the ion cyclotron frequency) as well as to plasma etching and to basic plasma physics.

Dr. Hershkowitz has a well-established record in helping postgraduate students, editing and refereeing important journals and in supporting the national fusion and basic plasma science program. He served as an Associate Editor of *Physics of Fluids* from 1981 to 1983 and has been a Divisional Associate Editor of *Physical Review Letters*. He is the Editor-In-Chief of *Plasma Sources—Science and Technology*, which began publication in February of 1992. In 1987, he received the IEEE Nuclear and Plasma Sciences Society Merdt Award. In 1993, he received the PSAC Award. He is a fellow of the APS. He was Chairman of the APS-Division of Plasma Physics from 1990 to 1991. He was also Chairman of the NPSS Awards Committee and past Vice-President of NPSS. Additionally, he has also served on the IEEE Nuclear and Plasma Sciences Society Administrative Committee. He currently is a member of the PSAC ExCom.

Soren Bisgaard holds two engineering degrees in industrial and manufacturing engineering and the M.S. and Ph.D degrees in statistics from the University of Wisconsin, Madison.

He is the Director at the Center for Quality and Productivity Improvement and an Associate Professor in the Department of Industrial Engineering, University of Wisconsin, Madison. Before entering the university, he worked for several years as a machinist and tool maker for companies in Denmark and Germany. He has worked as an industrial consultant in quality improvement and operations research, and has taught many short courses in statistical design of experiments and quality improvement methods. His primary research interest is in design of experiments and he has published more than 30 papers in refereed journals.

Dr. Bisgaard has received the Shewell Award three times and Brumbaugh Award two times from the American Society for Quality Control. In 1990, he received the Ellis R. Ott Award for excellence in quality improvement.



Shawming Ma (S'93) was born in Taipei, Taiwan, China. He received his B.S. degree in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1988. In 1991, he went to the United States for his graduate study and received M.S. degree in materials science and engineering in 1993 and the M.S. degree in electrical engineering in 1994 from Stanford University, Stanford, CA. He is currently pursuing the Ph.D. degree in materials science and engineering with a minor in electrical engineering at Stanford University.

He joined the Integrated Circuit Laboratory, Center of Integrated Systems, Stanford University, in 1993 under supervision of Sr. Research Scientist J. P. McVittie and Prof. K. C. Saraswat. His interests are in VLSI device physics and manufacturing technology, especially in plasma technology. Currently, he is working on charging induced device damage during plasma processings and development of SPORT (Stanford plasma on-wafer real time) charging probe as his Ph.D. dissertation.

James P. McVittie (M'75–SM'91) received the B.S. (EE) degree from the University of Illinois, Urbana-Champaign, in 1967 and the M.S. (EE) and the Ph.D. (EE) degrees in 1968 and 1972, respectively, from Stanford University, Stanford, CA.

He is a Senior Research Scientist in the Stanford University Center for Integrated Systems. From 1972 to 1974, he was a Member of the Technical Staff at the Lincoln Laboratory, Massachusetts Institute of Technology, Cambridge, where he worked on the growth of IV–VI compounds for laser diodes. In 1974, he joined the Xerox Palo Alto, CA, Research Center in the Device Physics Group where he worked on MOS interfaces and CCD's. He returned to Stanford in 1981 as a permanent member of the research staff in the Integrated Circuit Laboratory. Since 1985, he has headed a research group responsible for process development and modeling in CVD and plasma etch processes. Currently, the group is focusing on plasma charging, process induced device damage, and the development of SPEEDIE, which is the Stanford Profile Emulator for Etching and Deposition in IC Engineering. He has authored or co-authored more than 150 papers in the areas of plasma etching, CVD, metallization, oxidation, and semiconductor devices, and has given numerous invited papers on topography modeling and charging damage at international conferences.

Dr. McVittie is the recipient of the 1996 Tegal Thinker Award for outstanding work in plasma etching, a past chairman of the Northern California Chapter of the American Vacuum Society (1991), the Bay Area Plasma Etch User's Group (1989 to 1990), and of the Northern California Electronic Materials Symposium (1987). He has served on conference program committees for IEDM (1988 to 1989), SID (1989 to 1990), AVS (1993 to 1995).