Thin-oxide charging damage to microelectronic test structures in an electron-cyclotron-resonance plasma

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Processing yields in electron-cyclotron-resonance (ECR) and other high-density plasma sources will be increasingly limited by plasma-induced damage. This work investigates the effects of plasma nonuniformities on charging damage to polysilicon-gate MOS capacitor test structures exposed to O_2 ECR plasmas. The nonuniformities were produced by independently biasing electrodes located above the wafer. The damage was characterized with ramp-voltage breakdown measurements. Comparison of calculated profiles of the potential difference across the gate-oxide layers of the MOS capacitors with whole wafer maps of the breakdown voltage measurements shows that maximum damage occurs where the oxide potential difference is largest but only in the presence of plasma nonuniformities. © *1995 American Institute of Physics.*

The purpose of this work is: (i) to investigate charging damage to polysilicon-gate metal-oxide-semiconductor (MOS) capacitor antenna test structures upon exposure to O_2 plasmas generated in an electron-cyclotron-resonance (ECR) plasma source; and (ii) to determine the effect of radial plasma nonuniformities on the charging damage. Previous work with ECR reactors[1–3] and other types of plasma systems[4–7] has indicated that nonuniformities in the plasma parameters across the surface of the wafer during processing may play a role in the generation of charging damage. Our goal is to quantify the relationship between the plasma conditions and the degree of process-induced damage.

We will show that charging damage occurs when sufficiently large potential differences exist across the gate-oxide layers of the test structures. Also, it will be shown that these potential differences can only occur in the presence of plasma nonuniformities. The plasma parameters were characterized in terms of averages and standard deviations of profiles measured radially across the wafer surface. Charging damage was determined from ramp-voltage oxide-breakdown measurements of the MOS test structures.

The etching system employed here consists of a source region where high-density ECR plasma production is maintained, and a downstream processing region where the wafer is positioned. The source (ASTeX S-1500i, 1.5 kW 2.45 GHz) has a pair of magnets arranged in a magnetic-mirror configuration. The plasma parameters were measured with a Langmuir probe.[8] To modify the radial profiles of the plasma parameters, a dual-electrode assembly, oriented parallel to the wafer, consisting of a ring (10-cm diam) and a grid electrode (4.5 cm diam) which were independently biased, was mounted above the wafer stage. A diagram of the ECR system and dual-electrode assembly is shown in Fig. 1.

Charging of MOS capacitors produces potential differences across the gate oxide that cause Fowler–Nordheim (FN) tunneling currents[9,10] to flow through the gate-oxide layer which degrades the quality of the oxide and leads to breakdown. Such charging can result from local differences in the ion and electron current fluxes to the individual gates of the test structures.[6] To ascertain that charging is occurring, MOS capacitor antenna structures consisting of large area field-oxide capacitors in parallel with small area gate-oxide capacitors for which the ratio of the field-oxide area to the gate-oxide area is varied from 100 to 100 000 were used. Damage occurs when the exposed poly-Si electrode collects unbalanced plasma current and charges up to a potential where the thin gate oxide is then degraded by the fluence of the tunneling current.

Variation of the local charging conditions is seen by an examination of the floating-potential profiles. The floating potential (V_f) is the potential at which the ion and electron currents to the probe are equal.[8] Thus, it will vary in re-

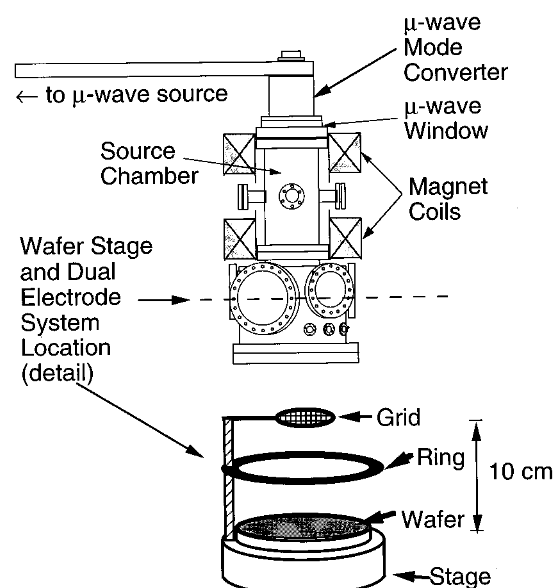

FIG. 1. A diagram of the ECR processing system and the dual electrode assembly.

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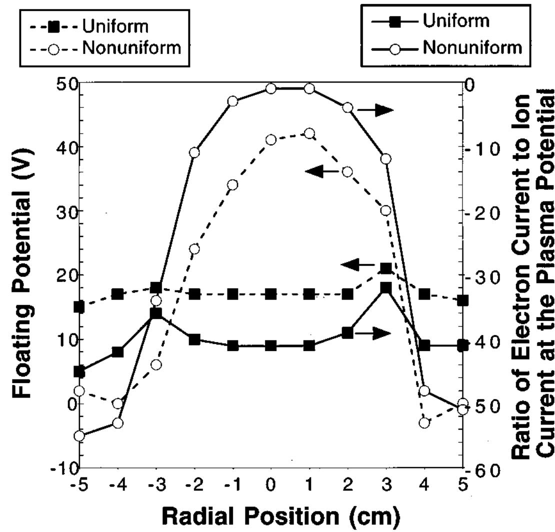

FIG. 2. Uniform and nonuniform floating potential profiles, generated with the dual electrode assembly, and corresponding electron to ion current ratio profiles. The operating settings (pressure, grid bias, and ring bias) of the dual-electrode assembly were (0.5 mTorr, 60 V, and −25 V) for the nonuniform profiles and (2.0 mTorr, 0 V, and +25 V) for the uniform profiles.

sponse to changes in these two current components.

Uniform and nonuniform V_f profiles created with the dual-electrode assembly are shown in Fig. 2. The (flat) uniform profile has an average of 17.1 V and a standard deviation of 1.5 V. For the nonuniform V_f profile these are 19.3 and 18.4 V, respectively.

The ratio of the electron current to the ion current at the plasma potential (I_e/I_i) is also plotted in Fig. 2. For the uniform I_e/I_i profile, the current ratio ranges from −31.6 to −44.8, and for the nonuniform profile the range of the ratio is from −1.4 to −55. 4.

The exponential dependence of the FN current on the voltage means that damage should map with oxide voltage with a sharp threshold dependent on the area ratio, oxide thickness, exposure time, and oxide quality of the test structures. For the case of no rf bias, the zero current condition corresponds to the surface being at the local floating potential as measured by a Langmuir probe. This leaves the silicon substrate voltage as the unknown needed to specify the voltage across the oxide.

During processing, a 50 W rf signal was applied to the wafer electrode. When a rf signal is capacitively coupled to the substrate, a rf self-bias develops across the coupling capacitor so that the total charge flow per cycle equals zero.[11] That is, the average value of the rf voltage shifts toward a negative potential so that the ion and electron currents to the substrate sum to zero over each rf cycle. The self-bias appears across the coupling capacitor, causing the potential on the surface of the wafer to shift in the direction of the self-bias potential. Because of the variation of the ion and electron currents across the wafer surface, nonuniform charging occurs.

The silicon substrate of the wafer has a low resistivity and can be considered an equipotential. In order to determine the potential of the substrate with respect to the surface of the wafer, consider the prebreakdown equivalent circuit of the test wafer and the electrode shown in Fig. 3. Each test structure is represented as a pair of capacitors, C_f and C_g, connected in parallel. V_{Si} is the potential of the silicon substrate with respect to ground and C_B represents the series capacitance of (i) the gap between the wafer and surface of the electrode, (ii) the anodized aluminum layer on the surface of the electrode, (iii) the rf blocking capacitor itself, and (iv) the tuning capacitors of the rf matching network. We call this series combination the blocking capacitor.

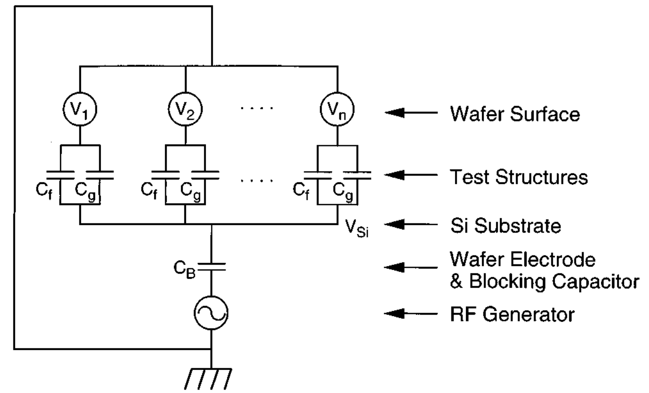

FIG. 3. Prebreakdown equivalent-circuit model of the test wafer and the wafer-stage electrode. The individual test structures are represented as the parallel network of the field-oxide capacitor C_f and the gate-oxide capacitor C_g. The voltage sources (V_i, $i=1-n$) for the test structures are needed to account for variations in the floating potential across the wafer surface. C_B is the blocking capacitor.

When the rf self-bias appears, charge flows into the blocking capacitor C_B, as well as into the individual test structures. Let the bias charge on the blocking capacitor be Q_B, and the bias charge on each individual test structure be Q_i. Because the blocking capacitor is in series with each test structure, the charge on the blocking capacitor (Q_B) must equal the sum of the charges on the individual test structures ($Q_1, Q_2, \ldots, Q_n$). That is, for the n test structures

$$Q_B = Q_1 + Q_2 + \cdots + Q_n. \quad (1)$$

In addition to the self-bias charge, variations in the potential across the surface of the wafer will result in additional charge flowing into some of the test structures. Referring to Fig. 3, each test structure has a specific surface potential feeding in charge. We represent these potentials as an array of voltage sources. The voltage source feeding test structure i has a value V_i which causes charge ΔQ_i to flow into that particular test structure as well as into C_B. Since C_B is in series with each test structure, the net charge ΔQ_B that accumulates in C_B is the sum of the additional charges on all of the individual test structures. Therefore, similar to Eq. (1), we write

$$\Delta Q_B = \Delta Q_1 + \Delta Q_2 + \cdots + \Delta Q_n. \quad (2)$$

Using Kirchoff's voltage law, we now sum the voltages around each loop of the circuit to yield

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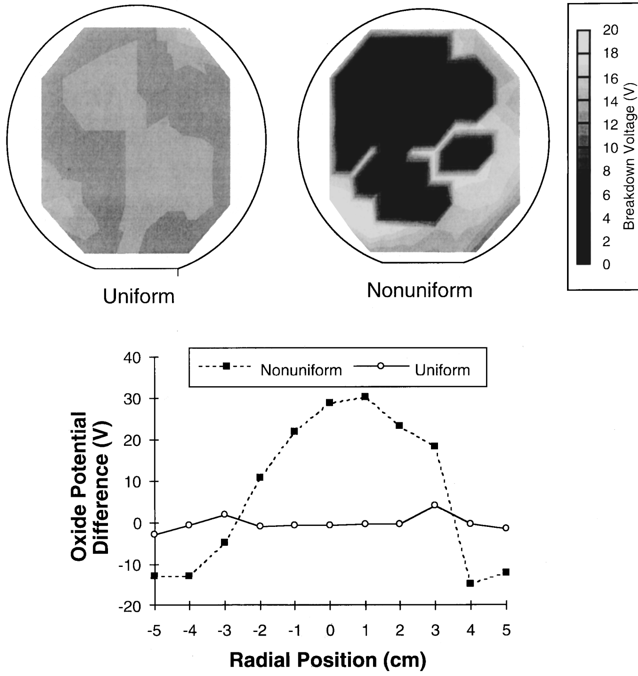

FIG. 4. Wafer maps of the breakdown voltages for test wafers exposed to uniform and nonuniform plasma conditions. The profiles of the calculated potential difference across the gate-oxide layer are also shown. The profiles were measured along a wafer diameter and angle of 75° counterclockwise with respect to the major wafer flat.

$$V_1 = \frac{Q_1+\Delta Q_1}{C_f+C_g}+V_{\text{Si}}, \tag{3}$$
$$\vdots \qquad \vdots$$
$$V_n = \frac{Q_n+\Delta Q_n}{C_f+C_g}+V_{\text{Si}}.$$

C is the parallel capacitance of each test structure ($C=C_f+C_g$). We sum these n equations to get

$$V_1+\cdots+V_n=\frac{Q_1+\Delta Q_1}{C}+\cdots+\frac{Q_n+\Delta Q_n}{C}+nV_{\text{Si}}, \tag{4}$$

or

$$\sum_{i=l}^{n} V_i=\left(\sum_{i=l}^{n} (Q_i+\Delta Q_i) \bigg/ C\right)+nV_{\text{Si}}. \tag{5}$$

Substituting Eqs. (1) and (2) gives

$$\sum_{i=l}^{n} V_i=\frac{Q_B+\Delta Q_B}{C}+nV_{\text{Si}}. \tag{6}$$

However, since $Q_B+\Delta Q_B=C_BV_{\text{Si}}$

$$\sum_{i=l}^{n} V_i=\frac{C_BV_{\text{Si}}}{C}+nV_{\text{Si}}=\left(\frac{C_B}{C}+n\right)V_{\text{Si}}. \tag{7}$$

Solving for V_{Si} yields the following expression for the potential of the silicon substrate:

$$V_{\text{Si}}=\frac{\Sigma_{i=l}^{n}V_i}{(C_B/C+n)}. \tag{8}$$

Equation (8) shows that V_{Si} is produced as the result of a series capacitive voltage dividing action between capacitors C_B and nC.

The average antenna structure capacitance C is 10 pF using a relative dielectric constant for SiO_2 of 3.9. The capacitance C_B is ~1 nF. Therefore, the ratio C_B/C is ≈100. Since the number of test structures (n) is on the order of 20 000, we can neglect the capacitance ratio C_B/C compared to n in the denominator of Eq. (8), so it becomes

$$V_{\text{Si}}=\frac{l}{n}\sum_{i=l}^{n} V_i. \tag{9}$$

Equation (9) shows that the potential of the silicon substrate is the average potential on the gates of the test structures. Since the test structures are distributed uniformly across the surface of the wafer, we approximate the potential of the silicon substrate as the average potential across the surface of the wafer.

For uniform potential profiles, Eq. (9) shows that the potential of the silicon substrate will be equal to the potential on the surface of the wafer, and the potential difference across the gate-oxide layers of the test structures will be small. If, on the other hand, the potential is nonuniform, Eq. (9) shows that the potential of the silicon substrate will be the average of the surface potential and relatively large potential differences can occur across the gate-oxide layers of the test structures. Profiles of the potential difference across the gate-oxide layer can be calculated assuming that the variation in the surface potential is the same as the variation of the floating-potential profile. The calculated gate-oxide potential profiles are shown in Fig. 4 together with area maps of the breakdown voltage for test wafers exposed to the same degree of plasma uniformity.

Thus we conclude that the potential of the silicon substrate is approximately equal to the average wafer surface potential. Therefore, when the wafer surface potential is uniform, the potential difference across the gate-oxide layers of the test structures will be small. Conversely, when the wafer surface potential is nonuniform, large potential differences can occur across the gate oxide resulting in charging damage.

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