An Investigation of the Effects of Iron in p^+n Silicon Diodes for Simulated Plasma Source Ion Implantation Studies

Kelly M. Brown, J. Leon Shohet, *Fellow, IEEE*, John H. Booske, Steven S. Gearhart, *Member, IEEE*, Henley L. Liu, *Student Member, IEEE*, Thomas G. Snodgrass, *Student Member, IEEE*, and R. R. Speth

***Abstract*—This work examines the effect of iron as a contaminate implant impurity on the characteristics of boron p^+n silicon diodes. Plasma-based doping processes [e.g., plasma source ion implantation (PSII)] are subject to concerns about the introduction of contaminant impurities. Here, a relevant database on iron contaminant effects was acquired through a controlled study using conventional ion-beam implantation. Uncontaminated control diodes had leakage current densities of 6–9 nA-cm^{-2} at -5 volts and ideality factors <1.05. Iron contaminated diodes had increasing leakage current densities of 8–60 nA-cm^{-2} with increasing iron implant doses of 4×10^7 to 4×10^{14} cm^{-2} and ideality factors <1.07 over six decades of current, regardless of dose.**

***Index Terms*— Boron, impurities, ion implementation, iron, leakage current.**

I. Introduction

A plasma-based doping process, such as plasma source ion implantation (PSII) [1] is a process in which a negative high voltage is applied to a substrate immersed within a plasma, causing ions to be accelerated toward the substrate. It has long been regarded as a possible alternative to classical ion-beam implantation, and research has been conducted concerning its use in semiconductor processing [2]–[5]. The benefits of PSII include low-energy/high-dose implants, lower implant cost, large implant area, and the absence of line-of-sight requirements. As device dimensions shrink and shallower junctions become more important [6], [7], these benefits are drawing more attention for use in integrated circuit fabrication. However, a general concern revolves around the implantation of unwanted contaminant ions into substrates and the potential effect on device characteristics and yield. Unwanted ions appear in the plasma due to the lack of a mass selection mechanism in PSII, as compared to classical ion-beam implantation. The unwanted ions can then be implanted into the device.

Experimenters have successfully fabricated diodes utilizing PSII [5]–[7], which resulted in near ideal forward currents with ideality factors <1.06 and leakage currents of 3–30 nA-cm^{-2} at -5 volts. These diodes were fabricated in a variety of plasma processing systems, obviously subject to different types and amounts of contaminates. To our knowledge, none of these experimenters established a correlation between increasing levels of a contaminate and the performance of a diode.

Now that the fabrication of devices using PSII has been shown possible, the next step is to determine the critical ratio of undesired to desired impurities above which results in devices that do not function adequately in comparison to those with no significant contamination. We experimentally simulate the contamination of boron p^+n silicon diodes, fabricated by PSII, by introducing boron as well as the contaminate impurity into the substrate using ion-beam implantation. We have chosen iron as the contaminate impurity since it is the most likely to be sputtered from the walls of a stainless steel vacuum chamber or wafer platform. In this work, however, we are constrained to implant the iron and boron separately, whereas in PSII both impurities are implanted simultaneously. In order to examine the effects of PSII as fully as can be done while using ion-beam implantation, half the runs were fabricated where the order of iron and boron implants was reversed, and a comparison of the characteristics of the diodes of both implant orders was made.

We used I–V measurements and subsequent analysis to determine the diode characteristics in the form of ideality factor, saturation current, generation rate of minority carriers, minority carrier lifetime of holes, and reverse-bias leakage-current density.

II. Experiment

Pretest diodes were fabricated at the Stanford Nanofabrication Facility (SNF), in Palo Alto, CA, and the Wisconsin Center for Applied Microelectronics (WCAM), a facility at the University of Wisconsin-Madison. The final fabrication for this study was conducted in WCAM, with the exception of the iron impurity implants. The various runs were fabricated over a two-month period and were therefore subject to uncontrolled

Manuscript received July 7, 1998; revised May 31, 1999. This work was supported in part by the National Science Foundation under Grant EEC-8721545.

K. M. Brown was with the Engineering Research Center for Plasma-Aided Manufacturing, Madison, WI 53706 USA. He is now with Seagate Technology, Bloomington, MI 55440 USA.

J. L. Shohet, J. H. Booske, S. S. Gearhart, H. L. Liu, and T. G. Snodgrass are with the Engineering Research Center for Plasma-Aided Manufacturing, Madison, WI 53706 USA.

R. R. Speth was with the Engineering Research Center for Plasma-Aided Manufacturing, Madison, WI 53706 USA. He is now with Intel Corp., Chandler, AZ 85225 USA.

Publisher Item Identifier S 0894-6507(99)08799-0.

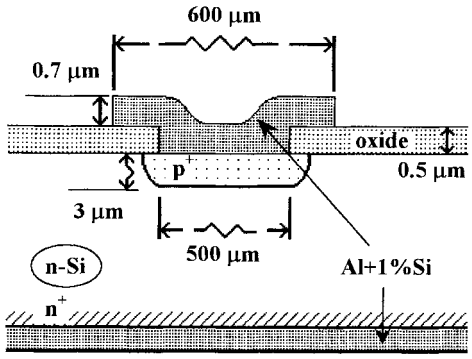


Fig. 1. Configuration of p^+n junction diode test structure.

TABLE I
BORON AND IRON IMPLANT ORDER AND RANGE OF IRON IMPLANT DOSE FOR EACH EXPERIMENTAL RUN

	Order of implant	*B (Ions/cm²)*	*Fe (Ions/cm²)*
Run 1	**B → Fe**	**$4x10^{15}$**	**$4x10^{8}$-$4x10^{13}$**
Run 2	**Fe → B**	**$4x10^{15}$**	**$4x10^{10}$-$4x10^{14}$**
Run 3	**Fe → B**	**$4x10^{15}$**	**$4x10^{7}$-$4x10^{14}$**
Run 4	**B → Fe**	**$4x10^{15}$**	**$4x10^{7}$-$4x10^{14}$**

process variations as a result of sharing multiuse fabrication tools.

The wafers used for the fabrication of all diodes were prime n-type silicon wafers, with $\langle 100 \rangle$ orientation, and resistivity of 1–10 Ω-cm. After the wafers were backside implanted with 1×10^{15} cm^{-2} of phosphorus and cleaned, 5000 Å of SiO_2 was grown on the wafers. The wafer test structures consisted of 500 μm diameter circular diodes, with an area of 1.96×10^{-3} cm^2. The diode contacts were 600 μm in diameter and located directly on top of the diodes as shown in Fig. 1.

Four runs were fabricated that all had boron implants of 4×10^{15} cm^{-2} using an energy of 60 keV and a 7° tilt. As shown in Table I, the iron implant doses ranged from 4×10^{7} to 4×10^{14} cm^{-2} for the same implant conditions. Run 1 consisted of six wafers having iron implantation doses between 4×10^{8} and 4×10^{13} cm^{-2} and where the boron was implanted into the substrates prior to the iron implant. Run 2 consisted of four wafers having iron implantation doses between 4×10^{10} and 4×10^{14} cm^{-2} and where the boron was implanted into the substrates after the iron implant. Run 3 consisted of eight wafers having iron implantation doses between 4×10^{7} and 4×10^{14} cm^{-2}. In run 3, the boron was also implanted into the substrates after the iron implant. Run 4 was identical to run 3 with the exception that the boron was implanted into the substrates prior to the iron implant. Two control wafers accompanied each run and were used as references in order to make a comparison of characteristics between contaminated and uncontaminated diodes.

Following both implantation steps, the wafers were annealed for 180 min at a temperature of 1100° C in a nitrogen atmosphere. Because of the presence of iron in the wafers, a designated furnace, referred to as the "metal-annealing" furnace, had to be used for the annealing of the metal-contaminated wafers. One uncontaminated wafer from each set was annealed in a high-purity process furnace, designated as the "metal-free" furnace, to determine if the metal-anneal furnace contributed any impurities to the substrate. The p^+n junction depth was predicted to be 3 μm. Simulations using Ssuprem3 [9] also indicated that the post-anneal iron concentration should be uniform throughout the wafer, due to the high diffusivity of iron in silicon at elevated temperatures. After the anneal, the wafers were cleaned, then 7000 Å of Al + 1% Si was sputter-deposited on the surfaces, followed by aluminum etching to define the diode contacts. All wafers were then annealed for 30 min at 450 °C in a nitrogen + 10% hydrogen atmosphere, to minimize interfacial traps.

III. CHARACTERISTICS OF DIODES

An HP4142B parameter analyzer was used to measure the I–V characteristics for all diodes. In order to compare the characteristics of the diodes, from wafer to wafer, the following parameters were calculated:

- n ideality factor;
- I_s saturation current (A);
- τ_G generation rate of minority carriers (s);
- τ_P minority carrier lifetime of holes (s);
- J reverse biased leakage-current density (A-cm^{-2}).

The ideality factor and saturation current were calculated by plotting the natural logarithm of the measured current $\ln(I)$ versus the applied voltage V_A and extrapolating the ideal region of the curve to the $\ln(I)$ axis. Taking the natural logarithm of the ideal-diode current equation gives

$$\ln(I) = \ln(I_s) + qV_A/nkT \tag{1}$$

where q is the electronic charge, n is the ideality factor, k is Boltzmann's constant, and T is the temperature. The intersection of this equation with the $\ln(I)$ axis is $\ln(I_s)$. The diode ideality factor was determined by finding the slope of the curve and equating it to q/nkT, the slope of (1). To calculate the generation rate of minority carriers, we used the following diode current density equations for a nonideal diode [11]:

$$J_R = q[D_p/\tau_p]^{1/2} n_i^2/N_D(\exp[qV_A/kT] - 1) - qn_iW/2\tau_G \tag{2}$$

$$J_F = q[D_p/\tau_p]^{1/2}(n_i^2/N_D)(\exp[qV_A/nkT] - 1) + qn_iW/2\tau_R(\exp[qV_A/2kT] - 1) \tag{3}$$

where the depletion width W is

$$W = [(2K_s\varepsilon_o/q)(V_{bi} - V_A)(N_A + N_D)/(N_AN_D)^{1/2} \tag{4}$$

and where J_R is the reverse-biased current density, J_F is the forward-biased current density, D_p is the diffusion constant of hole minority carriers, n_i is the number of intrinsic carriers, N_D is the number of majority carriers on the n-side of the junction, N_A is the number of majority carriers on the p-side of the junction, K_s is the dielectric constant of silicon, ε_o is

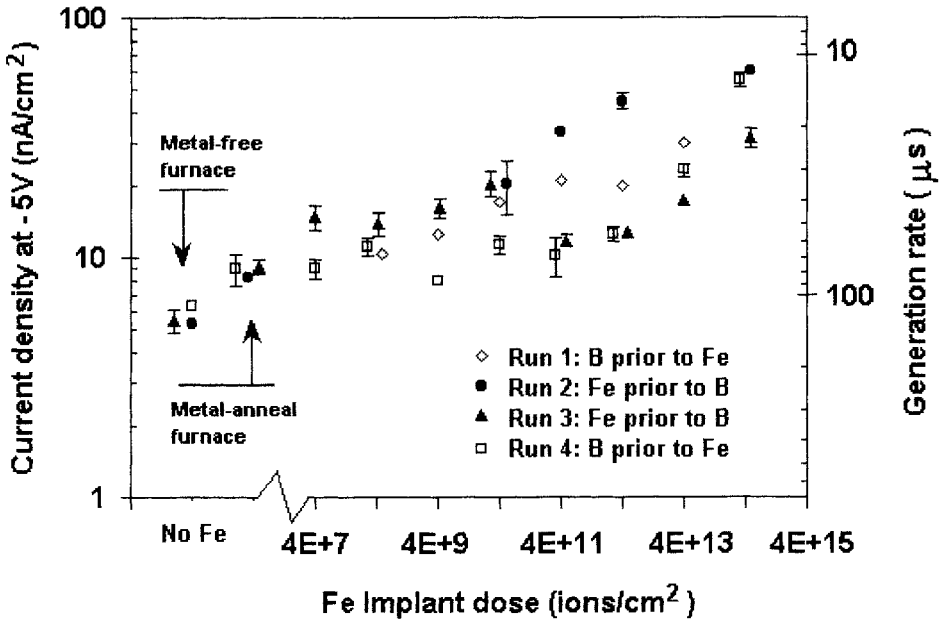


Fig. 2. Leakage-current density taken from I–V measurements at a reverse bias of -5 volts. Generation rate of minority carriers extracted from the current equation. Error bars display within-wafer variance. Sets 1 and 4 had boron implants prior to iron contamination implants. Sets 2 and 3 had iron implants prior to boron implants.

the permittivity of free space, and V_{bi} is the built-in voltage across the junction.

Equation (2) is the reverse-biased current-density equation. The first term on the right-hand side of (2) is the diffusion current of the diode. The second term is the current due to the generation of minority carriers in the depletion region, and it dominates the diffusion current for $V_A < 0$. By neglecting the diffusion term, the generation rate parameter τ_G can be solved for by using the measured current density in (2).

Equation (3) is the forward-biased current density equation. The first term on the right-hand side of (3) is the diffusion term. The second term is the current due to recombination of carriers in the depletion region. For very low voltages, $V_A < 0.2$ V, the recombination term dominates the diffusion term. For sufficiently larger voltages, $\sim$0.5 V, the diffusion term dominates, and by neglecting the recombination current in (3), the minority carrier lifetime of holes τ_P can be solved for using measured current density at V_A. τ_P will be used in the following equation to calculate the saturation current, where A is the area of the diode

$$I_s = qA[D_p/\tau_p]^{1/2} n_i^2/N_D. \tag{5}$$

The calculated saturation currents will then be compared with the saturation currents obtained experimentally.

IV. Results and Discussion

The effects of iron in silicon have been examined previously [12]–[15]. With various trapping levels reported throughout the band gap, we expected to see the leakage-current density increase with increasing iron dose. Examining Fig. 2, the leakage-current density at -5 volts was fairly constant for iron-implant doses of 4×10^{12} cm^{-2} and less. In general, there were no significant increases in leakage-current density until iron doses of 4×10^{13} cm^{-2} and greater were introduced. An exception was seen in two outlying points of run 2 at iron doses of 4×10^{12} and 4×10^{13} cm^{-2}, which was possibly the result of reworking run 2 at the sputter-deposition step of the diode fabrication process, where the aluminum was removed and redeposited. Another exception was seen in MOSFET studies by Pearce *et al.* [16], where they indicated leakage current densities independent of iron dosages up to 10^{15} cm^{-2}. However, their reported leakage current densities were greater than 3000 nA-cm^{-2}, two orders of magnitude greater than what we report here, and the iron implantation was into p-type substrates at 90 °C, while our work was performed on n-type substrates at room temperature.

Most of the wafers with iron doses in the range of 4×10^7 to 4×10^{12} cm^{-2} had diodes with leakage current densities of between 8 and 21 nA-cm^{-2}. This is comparable to work done by Qin and Chan [8], who produced plasma-doped p$^+$n diodes with leakage current densities of 15 nA-cm^{-2} at -5 volts for an iron contamination dose of 4.1×10^{12} cm^{-2}. Note that in [8], SIMS was used to detect the iron contaminate which came from the wafer platform. The wafers with iron doses of 4×10^{13} cm^{-2} had larger leakage current densities ranging from 17–30 nA-cm^{-2}. For an iron dose of 4×10^{14} cm^{-2}, the leakage-current density ranged from 31–60 nA-cm^{-2}, In work done by Vermeire *et al.*, significant increases in leakage current densities for contaminate doses $>1 \times 10^{13}$ cm^{-2} were also seen in their copper surface-contamination study [17]. The leakage current densities of the uncontaminated control diodes annealed in the metal-free furnace were $\sim$6 nA-cm^{-2}. The leakage current densities of the control diodes annealed in the metal-anneal furnace were $\sim$9 nA-cm^{-2}. Although it may not be statistically significant, this could indicate that some residual levels of unwanted impurities were introduced into

the iron-contaminated diodes during annealing in the metal-anneal furnace. In two of the four runs, iron was implanted into the wafers before boron. The diodes modified in this way had leakage currents comparable to those diodes fabricated with boron implanted first. This led us to the conclusion that for the purposes of implant doping with PSII, the simultaneous implanting of these impurities would yield similar leakage current densities.

The control diodes showed very little variability in the leakage current densities from run to run. The iron-contaminated diodes, however, showed some run-to-run variability with no clear trend in deviation. This variation can well be a result of fabrication inconsistencies due to sharing resources in the multi-user clean-room facility. The wafer anneals were confined to an anneal-furnace that is used for various metal anneals, and therefore any number of additional impurities were possibly introduced as a result.

By using the reverse-bias current-density (2), and neglecting the diffusion term, we can solve for the generation rate of minority carriers τ_G. The results corresponding to a given generation rate are seen on the right-hand side of Fig. 2. In conventional silicon processing, when the electron concentration is around 1×10^{15}–1×10^{16} cm^{-3}, the values of τ_G were between 2–200 μs [8], [18]. For the control diodes annealed in the metal-free furnace, the values of τ_G ranged from 109–130 μs. For the control diodes annealed in the metal-anneal furnace, the values of τ_G ranged from 75–82 μs. The iron contaminated diodes $> 4 \times 10^{13}$ cm^{-2} had much shorter values of τ_G which ranged from 11–40 μs. These small values of τ_G for high doses of iron are similar to the generation rates measured in iron-contaminated silicon using a MOS capacitor voltage/charge time-decay method [14].

The ideality factors and saturation currents are summarized in Table II. To calculate the saturation currents, we neglected the recombination term in (3) and solved for the minority carrier lifetime of holes τ_p. We used τ_p to solve for the saturation current in (5). The calculated saturation currents for both control wafers of each run were $\sim 0.5 \times 10^{-13}$ A. The calculated saturation currents of the iron-contaminated diodes for all implant doses ranged from 1.2×10^{-13} to 1.5×10^{-13} A. The control diodes annealed in the metal-free furnace had ideality factors <1.03, while the ones annealed in the metal-anneal furnace were <1.05. All the ideality factors of the iron-contaminated diodes were <1.07, which are less than values seen in another iron contamination study [15].

TABLE II
SATURATION CURRENT I_s AND IDEALITY FACTOR n FOR UNCONTAMINATED CONTROL DIODES DIFFUSED IN A METAL-FREE FURNACE AND IN A METAL-ANNEAL FURNACE, AND IRON CONTAMINATED DIODES DIFFUSED IN A METAL-ANNEAL FURNACE

	metal-free furnace	*metal-anneal furnace*	*metal-free furnace*	*metal-anneal furnace*
	I_s	I_s	n	n
Run 1				
Uncontaminated	—	—	—	—
Fe contaminated	—	**2.5-4.4x10^{-13}**	—	**1.04-1.06**
Run 2				
Uncontaminated	**1.0x10^{-13}**	**1.5x10^{-13}**	**1.03**	**1.05**
Fe contaminated	—	**1.8-9x10^{-13}**	—	**1.04-1.07**
Run 3				
Uncontaminated	**0.6x10^{-13}**	**1.3x10^{-13}**	**1.03**	**1.05**
Fe contaminated	—	**1-2.2x10^{-13}**	—	**1.02-1.04**
Run 4				
Uncontaminated	**1.0x10^{-13}**	**1.3x10^{-13}**	**1.01**	**1.03**
Fe contaminated	—	**1-3.5x10^{-13}**	—	**1.04-1.07**

V. SUMMARY

This work was motivated by the need to answer a concern about implanting unwanted impurities into devices during fabrication using plasma-based doping processes. The effect of iron as a contaminate implant impurity on the characteristics of p$^+$n silicon diodes was examined to determine at what dose devices would fail to function adequately. Iron-contaminated diodes with doses $<4 \times 10^{12}$ cm^{-2} were of good quality, generally yielding leakage-current densities of 8–21 nA-cm^{-2} at -5 volts. Leakage-current densities for all runs increased substantially with iron doses $>4 \times 10^{13}$ cm^{-2}. This study of iron contaminant effects in p$^+$n junction diodes is a useful step in dealing with the concern over unwanted impurities in PSII. With the many benefits accessible through PSII, which include low-energy/high-dose implants, lower implant cost, large implant area, and the absence of line-of-sight requirements, attention should continue to be placed on its use in integrated circuit fabrication.

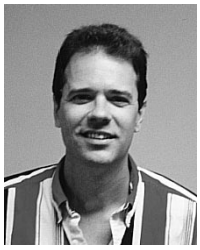
ACKNOWLEDGMENT

The authors would like to thank J. Shott at Stanford University for a grant that allowed them the use of the Stanford Nanofabrication Facility in Palo Alto, CA. Their thanks also go to P. Rissman, who is with Hewlett Packard Laboratories, Palo Alto, CA, for his helpful contributions and worthwhile discussions.

REFERENCES

[1] J. R. Conrad and J. L. Ratke, "Plasma source ion implantation technique for surface modification of materials," *J. Appl. Phys.*, vol. 62, pp. 4591–4596, Dec. 1987.
[2] C. Yu and N. W. Cheung, "Semiconductor processing with plasma implantation," *Nucl. Instrum. Methods Phys. Res.*, vol. B79, pp. 655–658, 1993.
[3] S. Qin, N. E. Gruer, C. Chan, and K. Warner, "Plasma immersion ion implantation doping using a microwave multipolar bucket plasma," *IEEE Trans. Electron Devices*, vol. 39, no. 10, pp. 2354–2358, 1992.
[4] N. W. Cheung, "Plasma immersion ion implantation for ULSI processing," *Nucl. Instrum. Methods Phys. Res.*, vol. B55, pp. 811–820, 1991.
[5] S. Qin and C. Chan, "Plasma immersion ion implantation doping experiments for microelectronics," *J. Vac. Sci. Technol. B*, vol. 12, pp. 962–968, Mar./Apr. 1994.
[6] E. C. Jones and N. W. Cheung, "Characteristics of Sub-100-nm p$^+$/m junctions fabricated by plasma immersion ion implantation," *IEEE Electron Device Lett.*, vol. 14, pp. 444–446, Sept. 1993.
[7] X. Y. Qian, N. W. Cheung, and M. A. Lieberman, "Plasma immersion ion implantation of SiF_4 and BF_3 for sub-100 nm P$^+$/N junction fabrication," *Appl. Phys. Lett.*, vol. 59, pp. 348–350, July 1991.
[8] S. Qin and C. Chan, "An evaluation of contamination from plasma immersion ion implantation on silicon device characteristics," *J. Electron. Mater.*, vol. 23, no. 3, pp. 337–340, 1994.
[9] Silvaco International, *SSUPREM3: 1-D Process Simulation*, Santa Clara, CA.

[10] C. E. Zah, "Millimeter wave-monolithic Schottky diode imaging arrays. Appendix B: Curve fitting for the measured I-V characteristics of Schottky diodes," Ph.D. dissertation, California Institute of Technology, Pasadena, CA., 1986, pp. 110–113.
[11] G. W. Neudeck, *The PN Junction Diode*. Reading, MA: Addison-Wesley 1989, ch. 4.
[12] K. Graff and J. Pieper, "The properties of iron in silicon," *J. Electrochem. Soc.*, vol. 128, no. 3, 1981.
[13] C. B. Collins and R. O. Carlson, "Properties of silicon doped with iron and copper," *Phys, Rev.*, vol. 108, no. 6, p. 1409, 1957.
[14] S. Naito and T. Nakashizu, "Electric degradation and defect formation of silicon due to Cu, Fe, and Ni contamination," *Mater. Res. Soc. Symp. Proc.*, Materials Research Society, vol. 262, 1992, pp. 641–652.
[15] L. K. Vandamme, E. P. Vandamme, and J. J. Dobblesteen, "Impact of silicon substrate, iron contamination and perimeter on saturation current and noise in n^+p diodes," *Solid-State Electron.*, vol. 41, no. 6, pp. 901–908, 1997.
[16] C. W. Pearce and R. J. Jacodine, "An analytical model of diffusion current in intrinsically gettered structures based on intentional contamination experiments," *IEEE Trans. Electron Devices*, vol. 38, no. 9, pp. 2155–2158, 1991.
[17] B. Vermeire, L. Lee, and H. G. Parks, "The effect of copper contamination on field overlap edges and perimeter junction leakage current," *IEEE Trans. Semiconduct. Manufact.*, vol. 11, pp. 232–237, May 1998.
[18] W. C. O'Mara, R. B. Herring, and L. P. Hunt, *Handbook of Semiconductor Silicon Technology*. Park Ridge, NJ: Noyes, 1990, pp. 564.



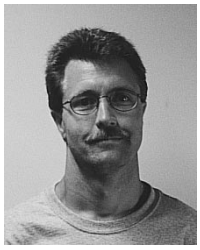
Kelly M. Brown received the B.S. degree in physics from Southwest Missouri State University, Springfield, in 1996 and the M.S. degree from the University of Wisconsin, Madison, in 1998.

In the summer of 1997, he worked at Hewlett-Packard Corporation in Santa Rosa, CA, dry etching, passivating, and testing GaAs PHEMT gate structures. He is currently employed at the Seagate Recording Heads Division in Bloomington, MN.

J. Leon Shohet (S'56–M'62–SM'72–F'78) received the Ph.D. degree in electrical engineering from Carnegie Mellon University, Pittsburgh, PA, in 1961.

He served on the faculty of Johns Hopkins University, Baltimore, MD, before joining the University of Wisconsin faculty in 1966 and was appointed Professor of Electrical and Computer Engineering in 1971. He is the Director of the Torsatron/Stellarator Laboratory, a major Department of Energy fusion research facility and is the Founding Director of the University's National Science Foundation Engineering Research Center for Plasma-Aided Manufacturing, as well as the past Chairman of the Department of Electrical and Computer Engineering. He is the author of two textbooks on plasma science, over 130 journal articles, and more than 400 conference papers. He holds seven patents. His research interests are: plasma-aided manufacturing; fusion, especially waves, instabilities, heating, confinement, and diagnostics; plasma-aided manufacturing; communications; magnetohydrodynamics; electromagnetic field theory; biophysics; and quantum electronics and lasers.

Dr. Shohet is a Fellow of the American Physical Society. He received the Frederick Emmons Terman award of the American Society for Engineering Education, the Merit Award of the IEEE's Nuclear and Plasma Sciences Society, the IEEE Richard F. Shea Award, the IEEE Plasma Science Prize, the IEEE Centennial Medal and the John Yarwood Memorial Medal from the British Vacuum Council. He founded the IEEE TRANSACTIONS ON PLASMA SCIENCE in 1973.



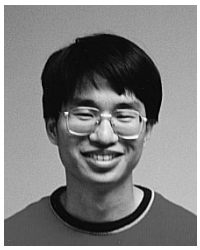
John H. Booske received the Ph.D. degree in nuclear engineering from the University of Michigan, Ann Arbor, in 1985.

He is a Professor of Electrical and Computer Engineering at the University of Wisconsin, Madison, having joined the faculty in 1990. Between 1985–1989, he worked at the Laboratory for Plasma Research, University of Maryland, College Park. His research interests include microwave vacuum electronics, microwave processing of materials, and plasma modification of materials surfaces.

Steven S. Gearhart (S'91–M'95) received the B.S.E.E. degree from Virginia Polytechnic Institute and State University, Blacksburg, in 1988 and the M.S.E.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1990 and 1994, respectively.

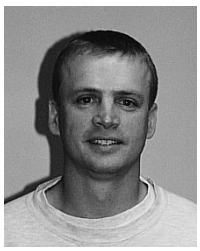
Since 1994, he has been an Assistant Professor in the Department of Electrical and Computer Engineering at the University of Wisconsin, Madison. His research interests include micromachined integrated circuits and antennas, polarization-agile and multi-resonant antenna elements, automotive radar systems, and silicon ultra-shallow CMOS junctions.

In 1998, Dr. Gerhart received the Army Research Office Young Investigator Award.



Henley L. Liu (S'97) received the B.S. degree from National Taiwan University in 1991, and the M.S. degree from the University of Wisconsin, Madison in 1995, both in electrical engineering. He is currently pursuing the Ph.D. degree in electrical and computer engineering at the University of Wisconsin, Madison.

His research interests include deep sub-micron MOSFET technology and other exploratory devices.



Thomas G. Snodgrass (S'96) received the B.S. degree in physics and the M.S. degree in mathematics from the University of Nebraska, Lincoln, in 1991 and 1994, respectively. He is currently pursuing the Ph.D. degree in electrical and computer engineering at the University of Wisconsin, Madison.

From 1990 to 1991, he had internships at the University of Colorado, Boulder, Argonne National Laboratories, and Sandia National Laboratories.

R. R. Speth, photograph and biography not available at the time of publication.